Compal Confidential

PAGANI M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point

Date : 2011/11/22
Version 0.1

Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title	Block Diagrams	
Size: Custom	Document Number: LA-8711	Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 1 of 57	

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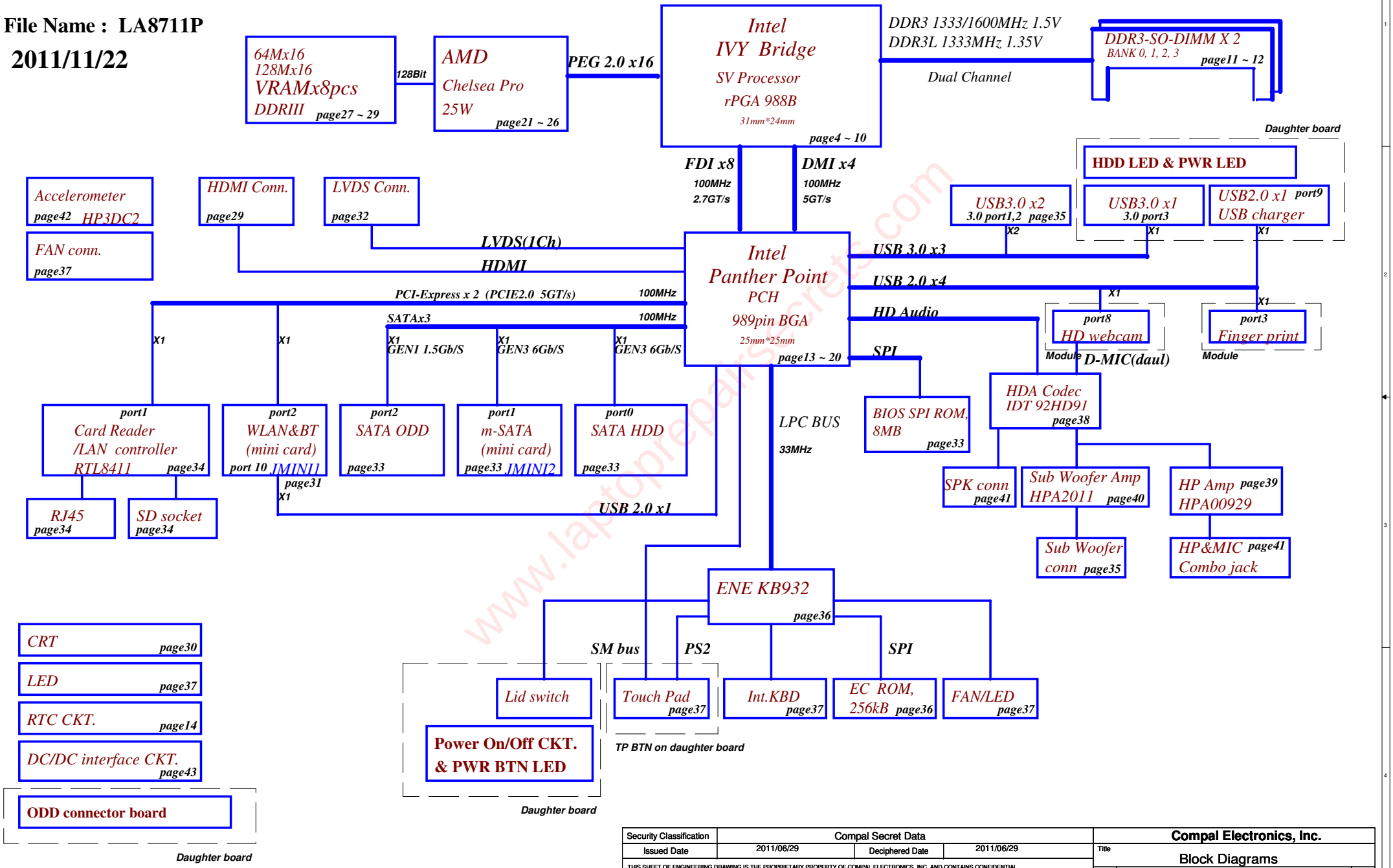
Model Name : Zonda

File Name : LA8711P

2011/11/22



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Compal Electronics, Inc.

Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_VDD_3V3	+3VALW to +LAN_VDD_3V3 power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
G-sensor	0101001b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	BATT Charger	TP	SODIMM	EC_SMB_CK2 EC_SMB_DA2	PCH_SML1CLK PCH_SML1DATA	G-Sensor	GPU	HP AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V		V					V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	
PCH_SMBCLK PCH_SMBDATA	PCH				V	V					V
PCH_SML0CLK PCH_SML0DATA	PCH										
PCH_SML1CLK PCH_SML1DATA	PCH						V				

SATA	DESTINATION
SATA0	HDD,JHDD1
SATA1	m-SATA,JMINI2
SATA2	ODD, JODD1
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	USB3.0
		1	USB3.0
	UHCI1	2	USB3.0
		3	USB2.0 FRP
	UHCI2	4	X
		5	m-SATA
	UHCI3	6	X
		7	X
EHCI2	UHCI4	8	Camera
		9	USB2.0 and sleep charger
	UHCI5	10	minPCIE-WLAN/BT
		11	X
	UHCI6	12	X
		13	X

USB 3.0	Port	3 External USB Port
	0	USB3.0
	1	USB3.0
	2	USB3.0(SB)

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	CR+ Giga LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

Option	@	CONN@	PX@	
UMA	X	X	X	
DIS	X	X	V	

Symbol Note :

: means Digital Ground

: means Analog Ground

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Title	Notes List		
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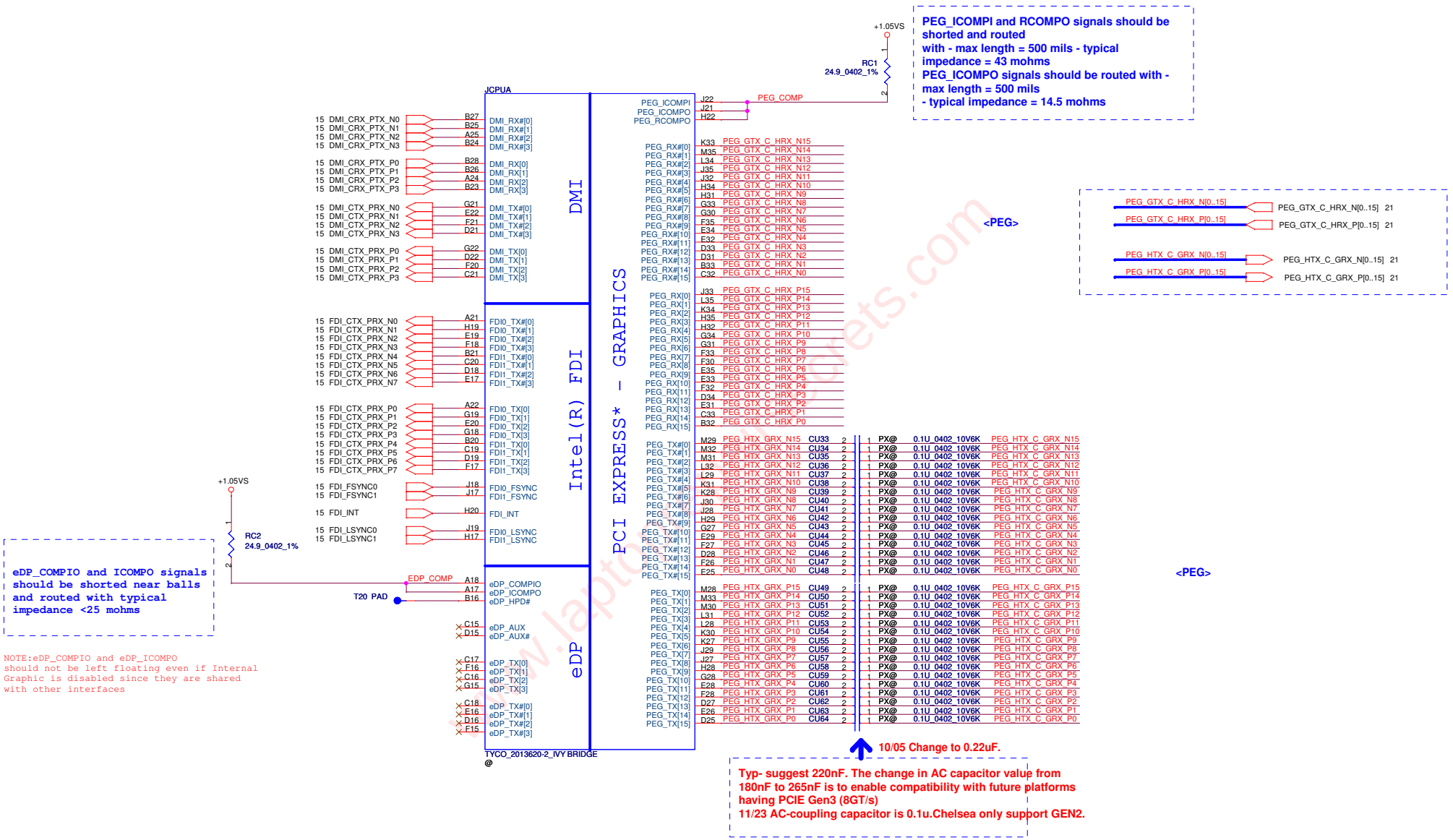

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Compal Electronics, Inc.			
Title	PROCESSOR(1/7) DMI,FDI,PEG		
Size: Custom	Document Number: LA-8551P		Rev: 0.1
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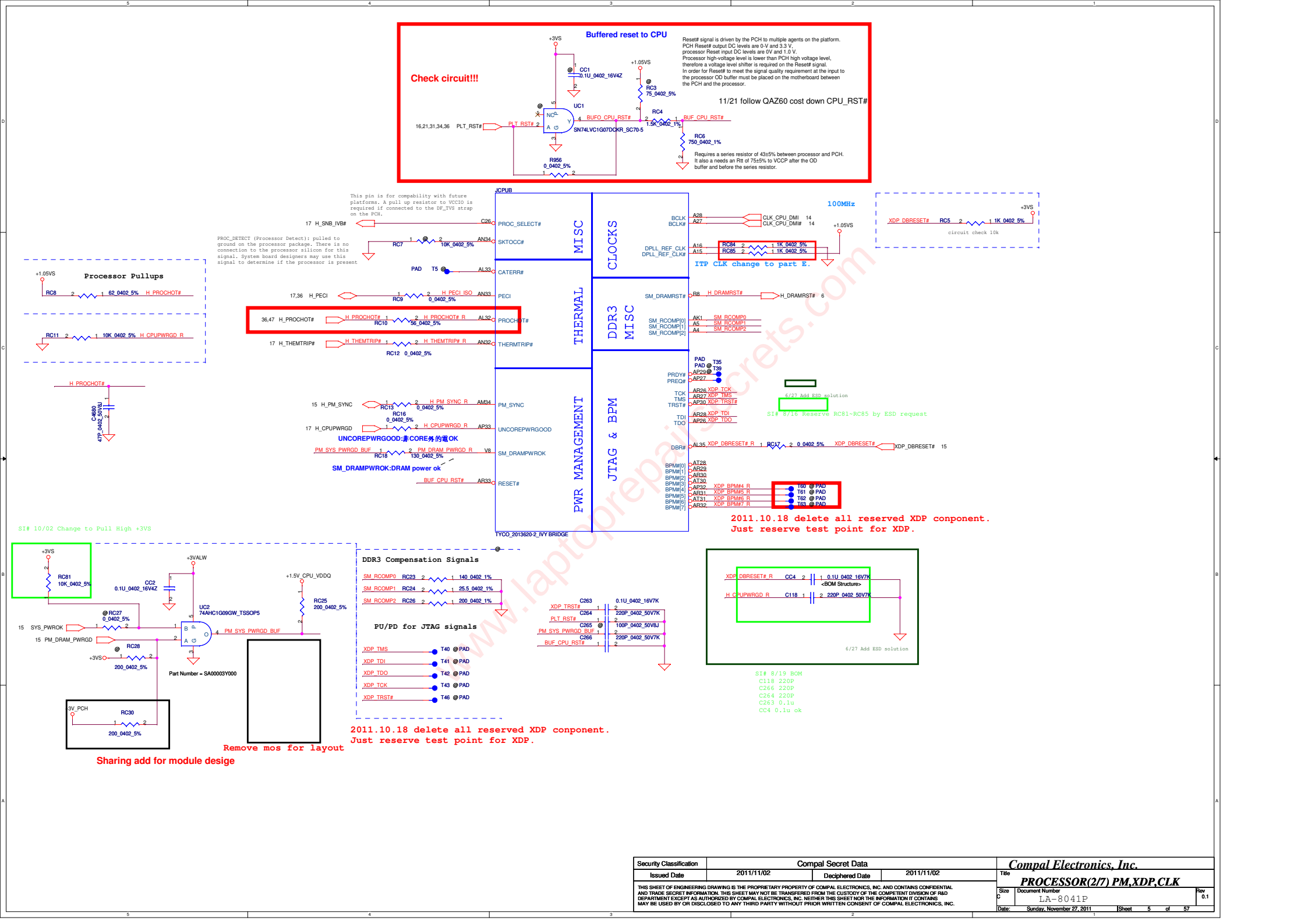

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Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: PROCESSOR(2/7) PM,XDP,CLK

Size	Document Number	Rev
C	LA-8041P	0.1

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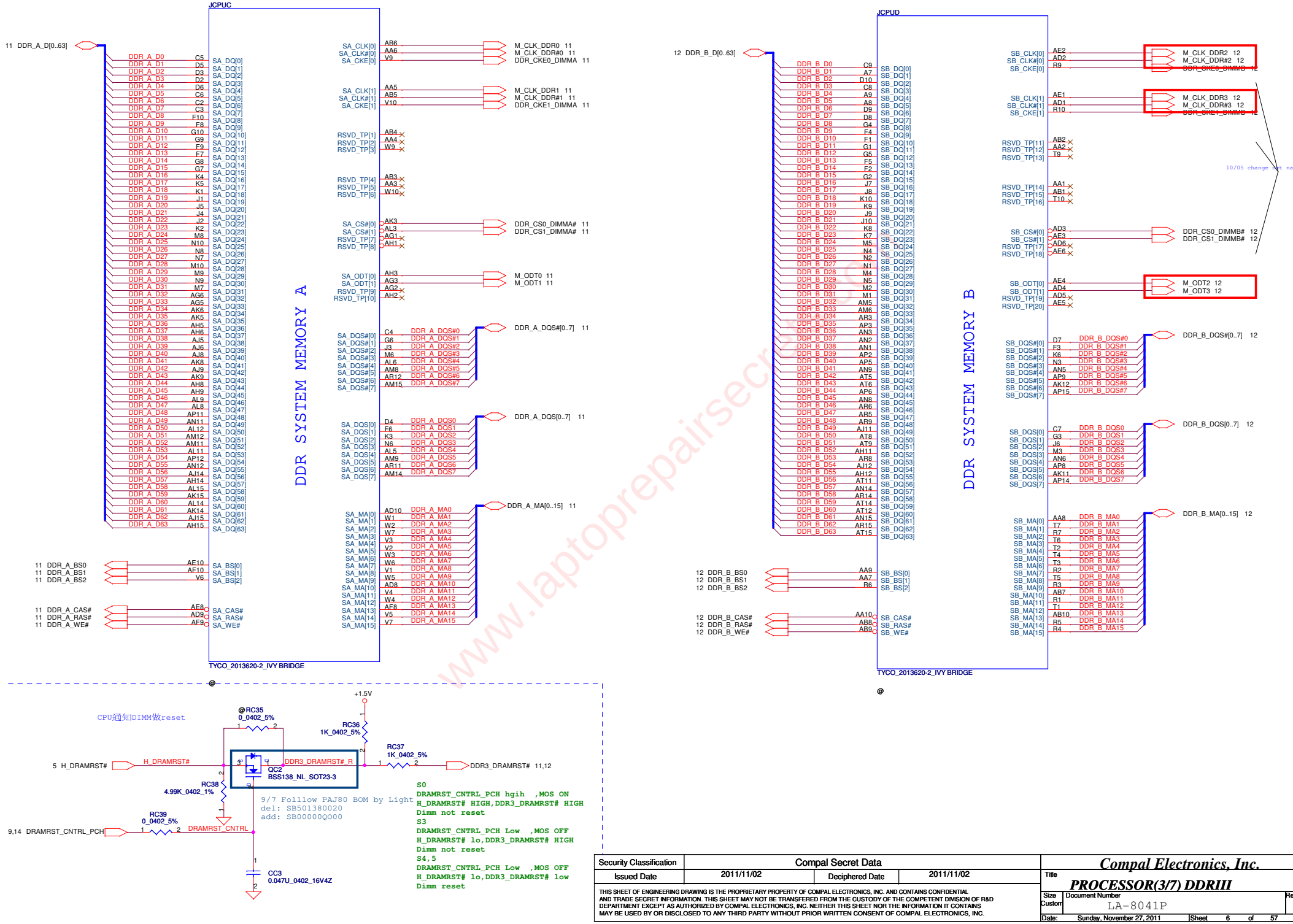

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Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	LA-8041P	0.1

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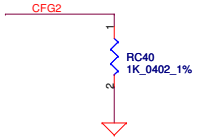
CFG Straps for Processor

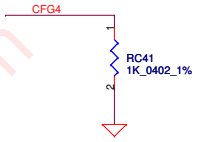
Change to part G.

change to install

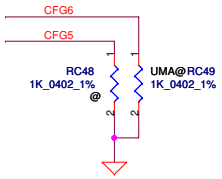


PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

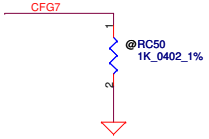
change to install



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled *01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

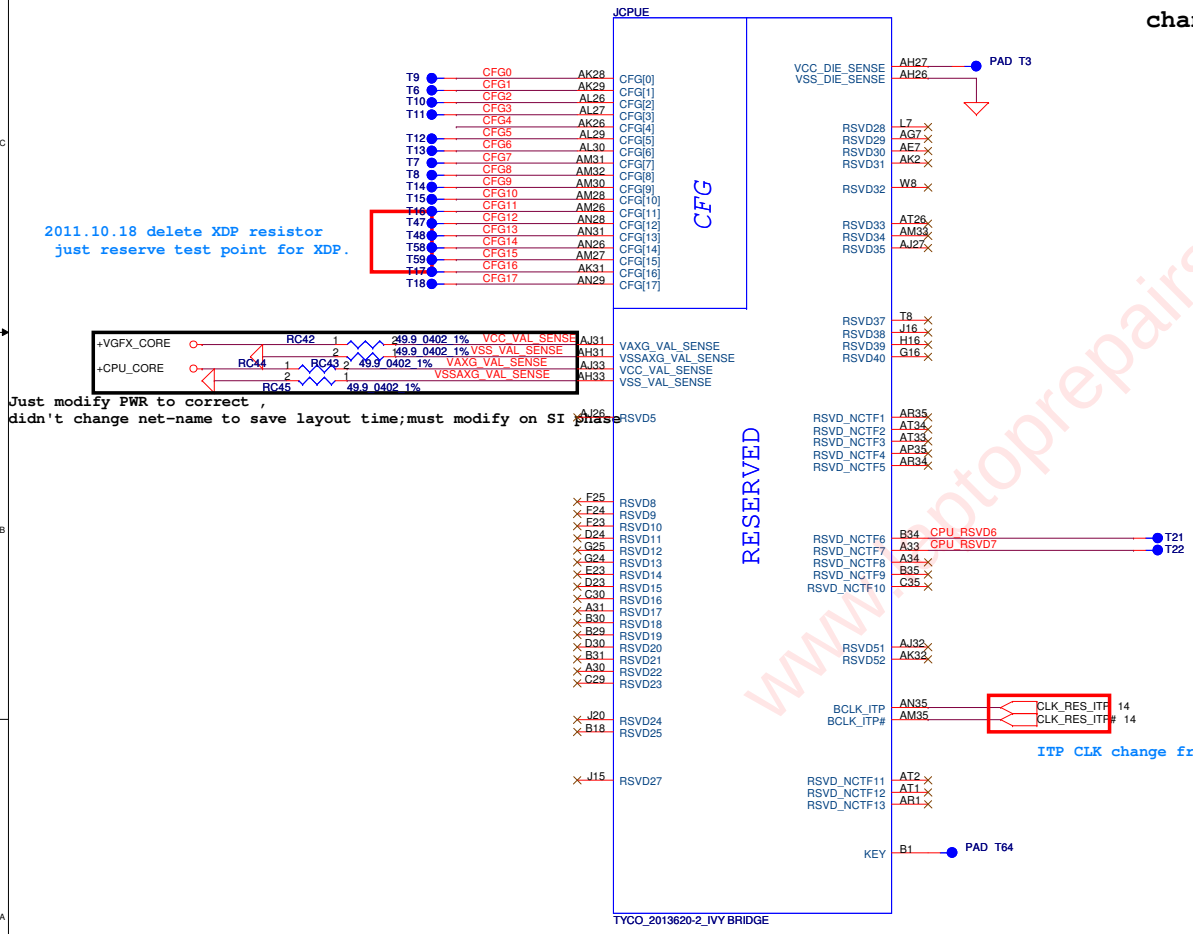


PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

2011.10.18 delete XDP resistor
just reserve test point for XDP.

Just modify PWR to correct ,
didn't change net-name to save layout time;must modify on SI phase

ITP CLK change from part C.



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Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
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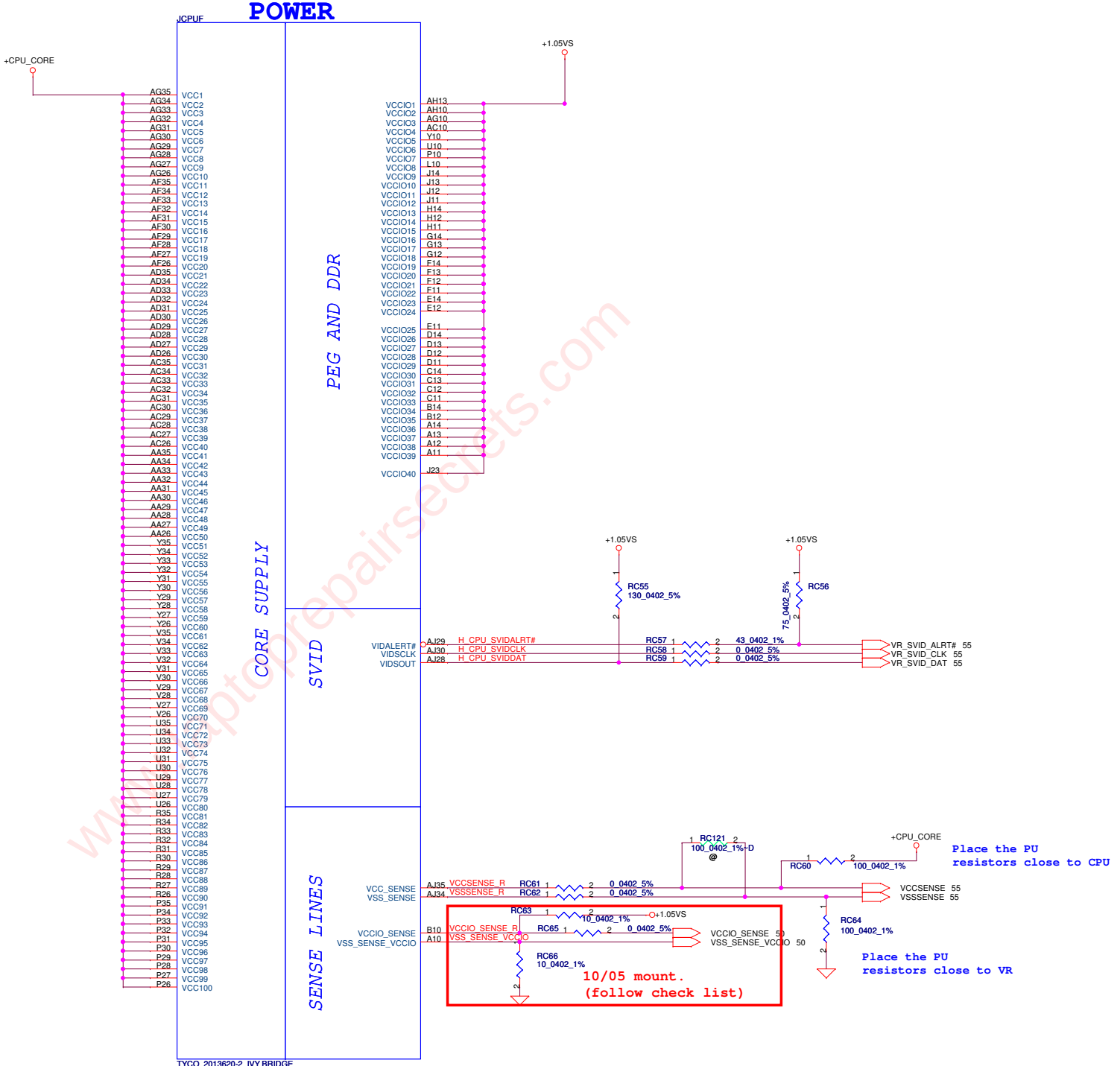
POWER



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Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

Size	Document Number	Rev
Custom	LA-8041P	0.1

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- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

POWER

+1.5V_CPU_VDDQ
CC74 2 1 0.1U_0402_10V7K
CC75 2 1 0.1U_0402_10V7K
+1.5V

+VGFX_CORE

JCPUG

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36 VAXG37 VAXG38 VAXG39 VAXG40 VAXG41 VAXG42 VAXG43 VAXG44 VAXG45 VAXG46 VAXG47 VAXG48 VAXG49 VAXG50 VAXG51 VAXG52 VAXG53 VAXG54

GRAPHICS

SENSE LINES
VAXG_SENSE AK35
VSSAXG_SENSE AK34
RC157 1 @ 2 100_0402_1%~D
100±5% pull-up to VCC;
100±5% pull-down to GND.
VCC_AXG_SENSE 55
VSS_AXG_SENSE 55
+V_SM_VREF should have 20 mil trace width

VREF
SM_VREF AL1
+V_SM_VREF_CNT
CC79 0.1U_0402_16V4Z
SA_DIMM_VREFDQ B4 +V_DDR_REFA_R
SB_DIMM_VREFDQ D1 +V_DDR_REFB_R

DDR3 -1.5V RAILS
VDDQ1 AF7
VDDQ2 AF4
VDDQ3 AF1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

SA RAIL
VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

MISC 1.8V RAIL
VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2
VCCSA_SENSE H23
VCCSA_VID[0] C22
VCCSA_VID[1] C24
VCCIO_SEL A19
TYCO_2013620-2_IVY BRIDGE

+1.5V_CPU_VDDQ
RC68 1K_0402_1%
RC69 1K_0402_1%
11/21 follow PBL22 design remove 10u*2, 1U*8; keep 10U*5
CC100 330U_D2_2V_Y
+1.5V_CPU_VDDQ Source

QC4 Change to SA0000JA00 for small package 1016

+VCCSA
CC22 10U_0603_6.3V6M
CC21 10U_0603_6.3V6M
CC24 10U_0603_6.3V6M
Delete CC25 330U cap 10.19 (after check with power)
11/21 follow PBL22 design remove 10u*2, 1U*5

VCCSA_SENSE 52
RC78 @ 0_0402_5%
+1.05VS
RC79 0_0402_5%
VCCSA_VID0 52
VCCSA_VID1 52
RC80 0_0402_5%
RC52 @ 75_0402_5%
VCCP_PWRCTRL_R
RC53 @ 10K_0402_5%

CPU EDS descript as follow:
For Chief River platforms this pin should not be used.

+1.8VS
RC77 0_0805_5%
+1.8VS_VCCPLL
CC29 10U_0603_6.3V6M
CC120 @ 330U_D2_2VM_R6M
CC121 1U_0402_6.3V6K
CC122 1U_0402_6.3V6K
SI# 7/29 Add CC26 10uF and reserve 330U on 1.8V power Rail

For Chief River only

M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

QC7 SB000002X00 BSS138W-7-F_SOT323-3
DRAMRST_CNTRL_PCH
DRAMRST_CNTRL_PCH 6,14
+V_DDR_REFA
RC15 @ 0_0402_5%
+V_DDR_REFA_R
RC14 @ 1K_0402_1%

QC8 SB000002X00 BSS138W-7-F_SOT323-3
DRAMRST_CNTRL_PCH
+V_DDR_REFB
RC82 @ 0_0402_5%
+V_DDR_REFB_R
RC83 @ 1K_0402_1%

10/03 add +V_DDR_REFB

+3VALW
+VSB
RC70 100K_0402_5%
RC72 100K_0402_5%
RUN_ON_CPU1.5VS3
RC74 0_0402_5%
36 CPU1.5V_S3_GATE
@RC75 0_0402_5%
36,43,50,51,52,53 SUSP#
2N7002DWH_SOT363-6 QC5B
2N7002DWH_SOT363-6 QC5A

+1.5V
QC4 AON6718L_DFN8-5
+1.5V_CPU_VDDQ
RC71 470_0603_5%
R78 @ 20K_0402_5%
RC73 330K_0402_5%
CC118 0.1U_0402_25V6
Q10A 2N7002DWH_SOT363-6
RUN_ON_CPU1.5VS3#
SI# BOM Change CC118 0.1u 25V form 0.1u 16V

VID[0]	VID[1]		2011	2012
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

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Title: PROCESSOR(6/7) PWR

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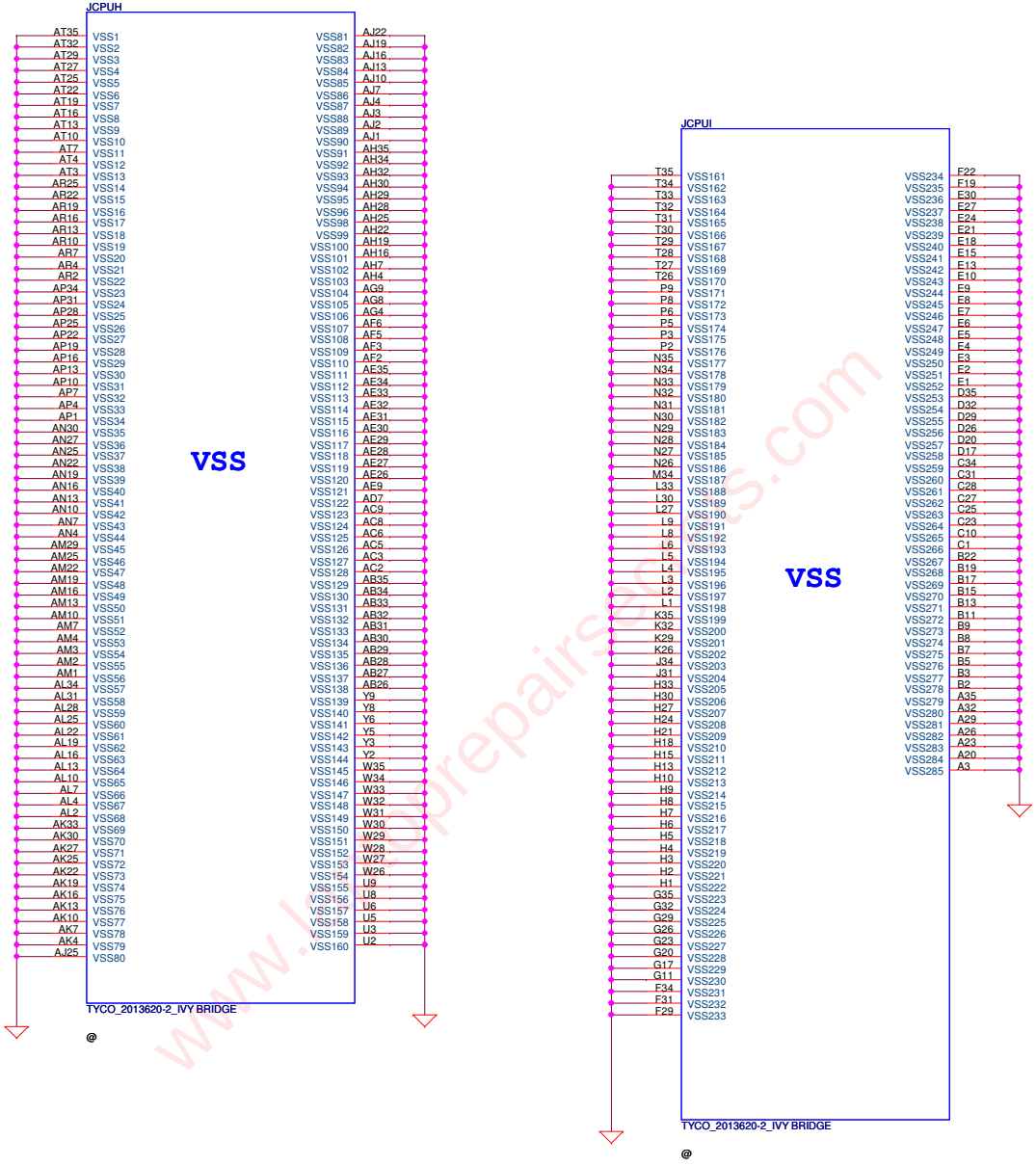

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Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size	Document Number	Rev
Custom	LA-8041P	0.1

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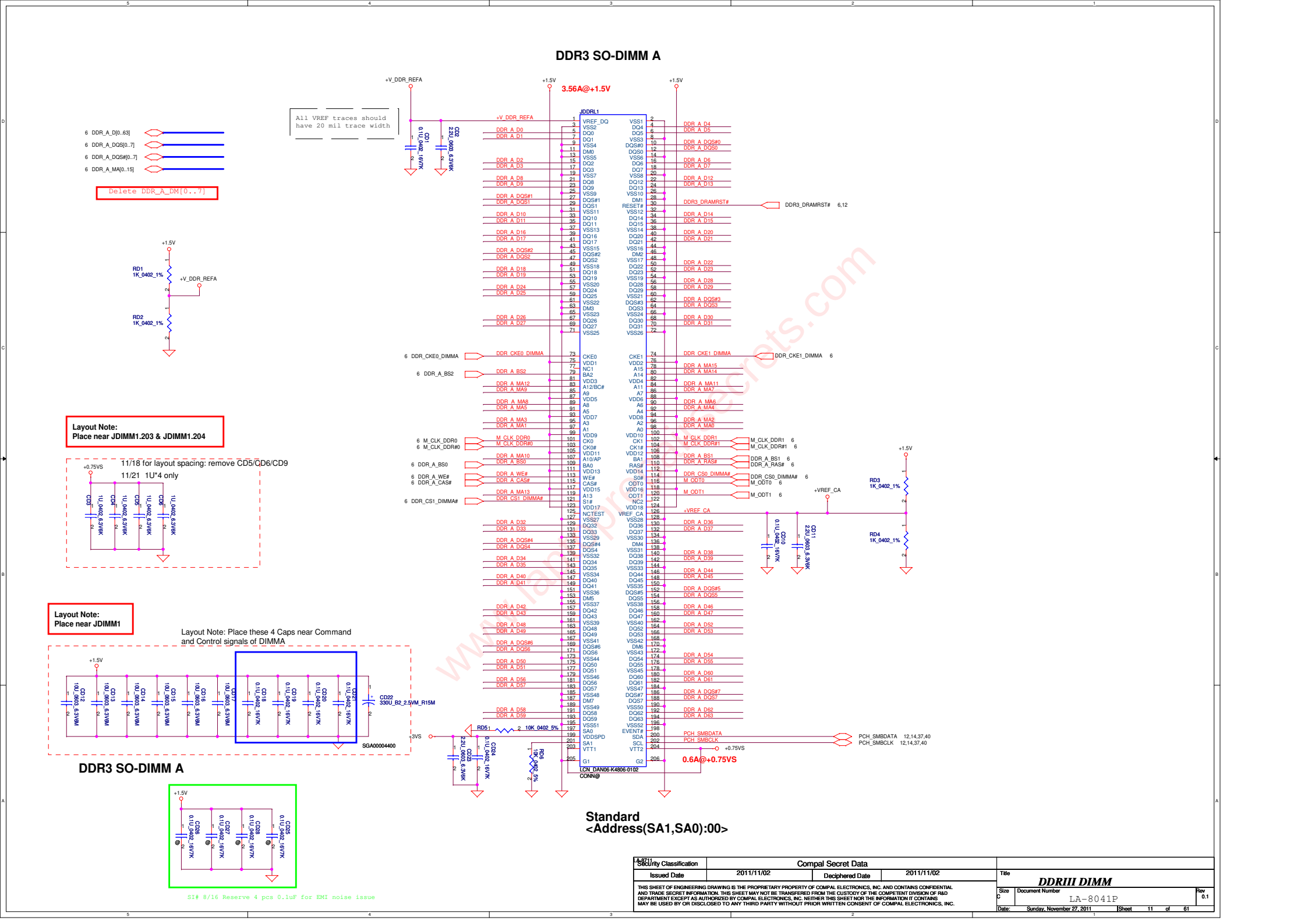
DDR3 SO-DIMM A



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Title	DDRIII DIMM		
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DDR3 SO-DIMM B

10/03 change to +V_DDR_REFB

3.56A@+1.5V

All VREF traces should have 20 mil trace width

6 DDR_B_D[0..63]
6 DDR_B_DQS[0..7]
6 DDR_B_DQS#[0..7]
6 DDR_B_MA[0..15]

Delete DDR_B_DM[0..7]

RD12 1K_0402_1%
RD11 1K_0402_1%

10/03 change to +V_DDR_REFB

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

11/18 for layout spacing: remove CD51/CD54/CD53
11/21 keep 1u*4 only -Kenny

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

CD36 330U_B2_2.5VM_R15M
SGA00004400

DDR3 SO-DIMM B

SI# 8/16 Reserve 4 pcs 0.1uF for EMI noise issue

JDDRL2
LCN_DAN06-K4406-0102
CONN@

10/03 change to +VREF_CB

10/05 change to PH.

Standard
<Address(SA1,SA0):10>

0.6A@+0.75VS

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Title: DDRIII-DDRH

Size	Document Number	Rev
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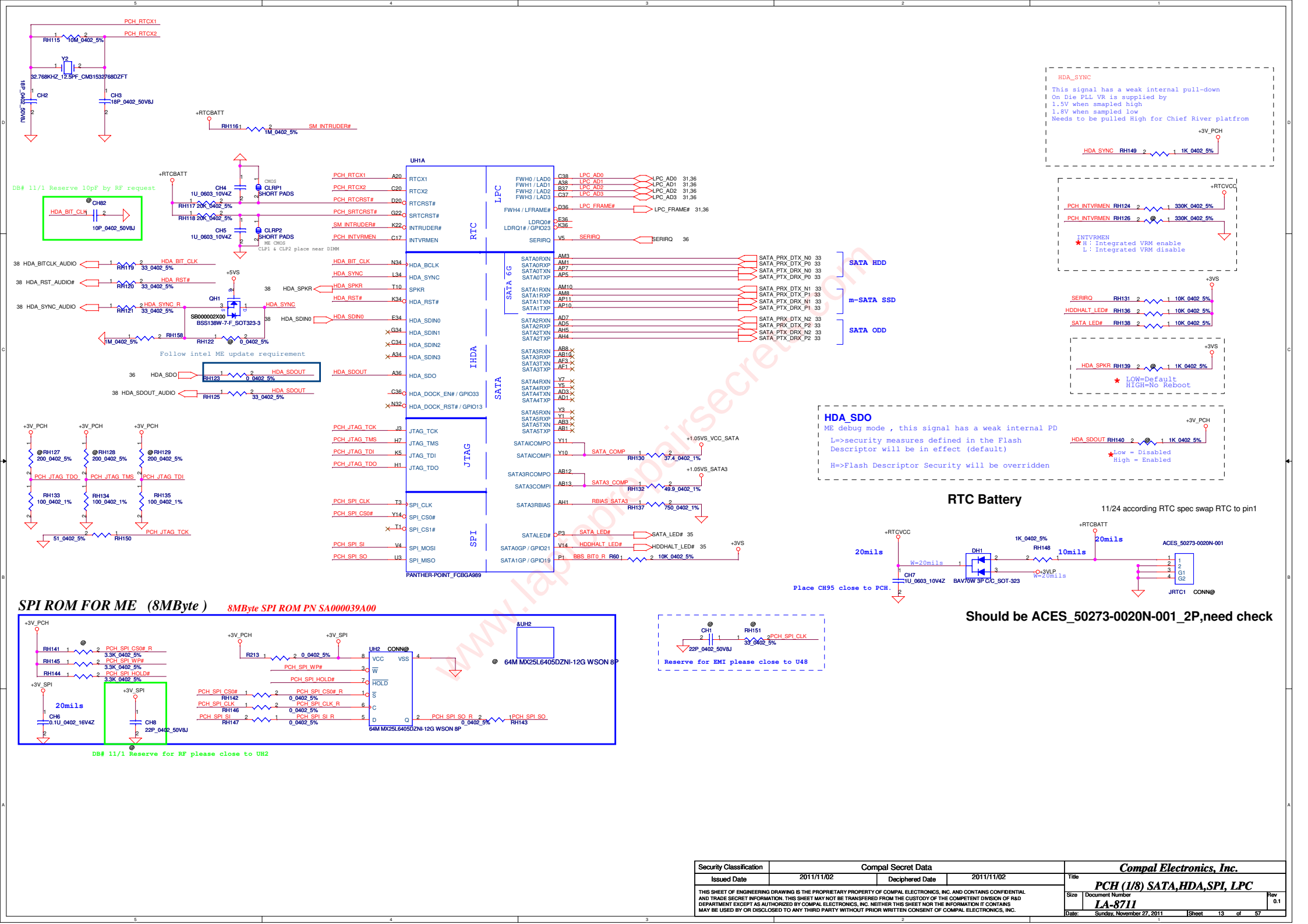

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.	
Title	PCH (1/8) SATA,HDA,SPI, LPC
Size	Document Number: LA-8711
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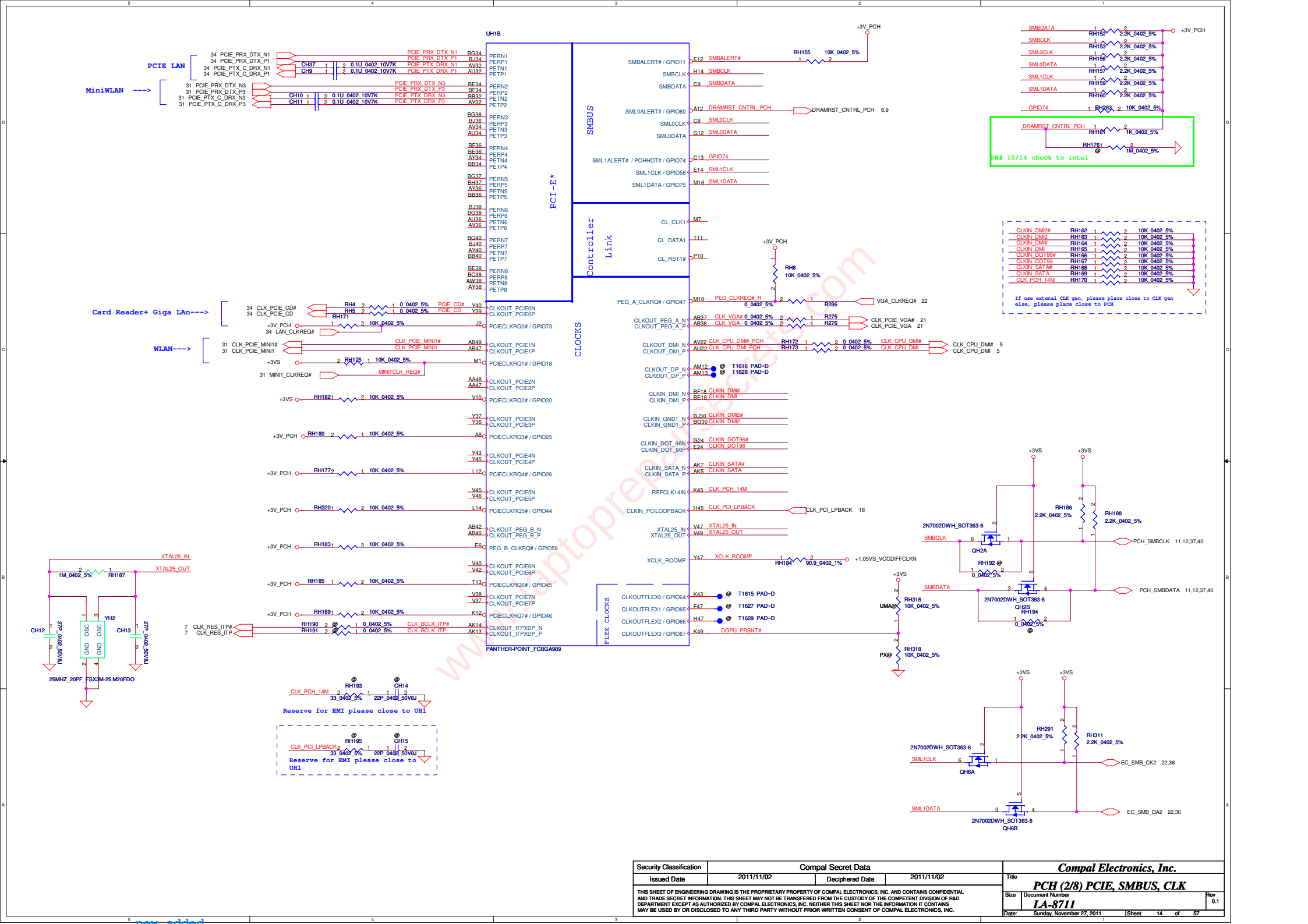

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Compal Electronics, Inc.

Title: **PCH (2/8) PCIE, SMBUS, CLK**

Size	Document Number	Rev
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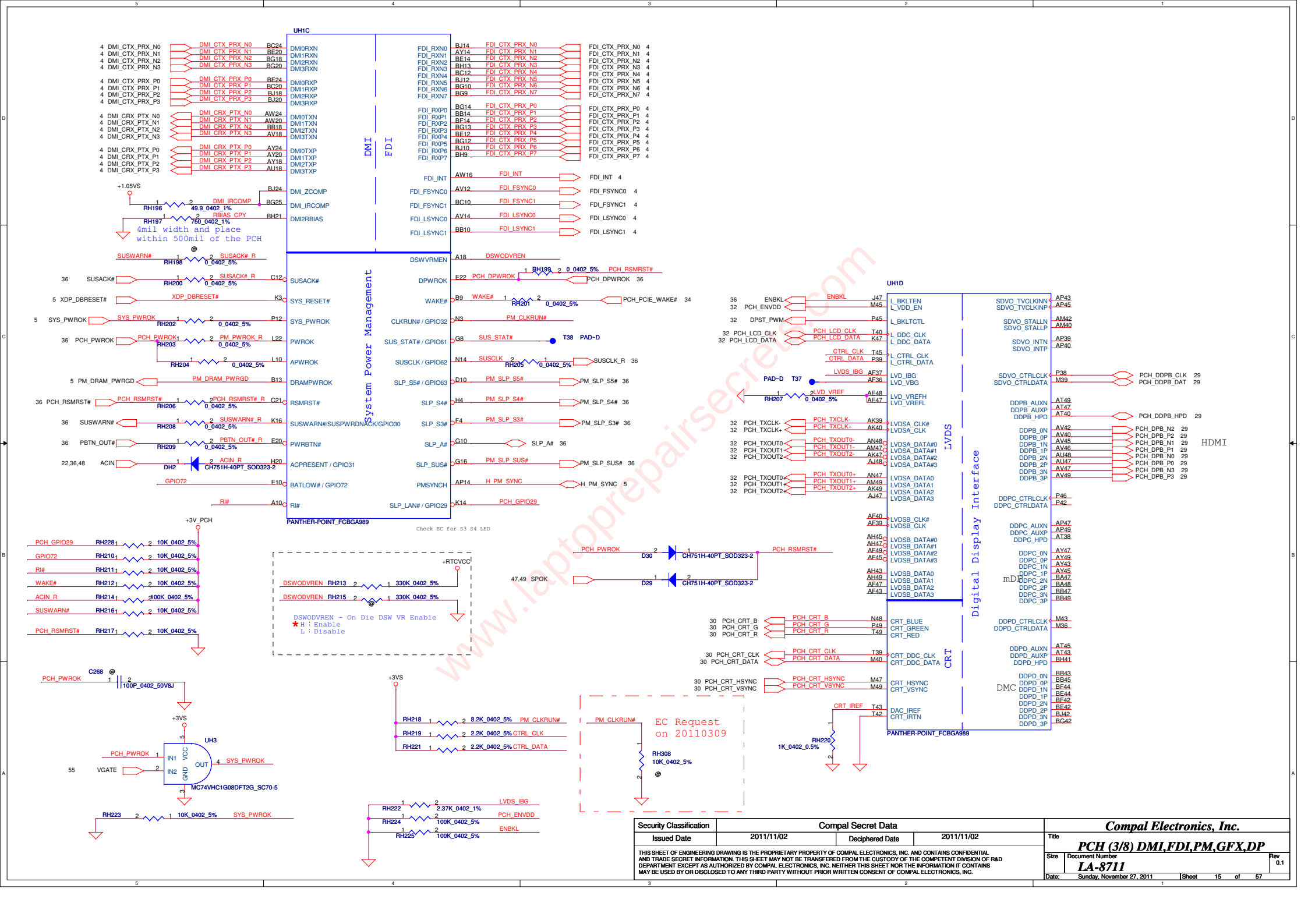

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **PCH (3/8) DMI,FDI,PM,GFX,DP**

Size	Document Number	Rev
	LA-8711	0.1

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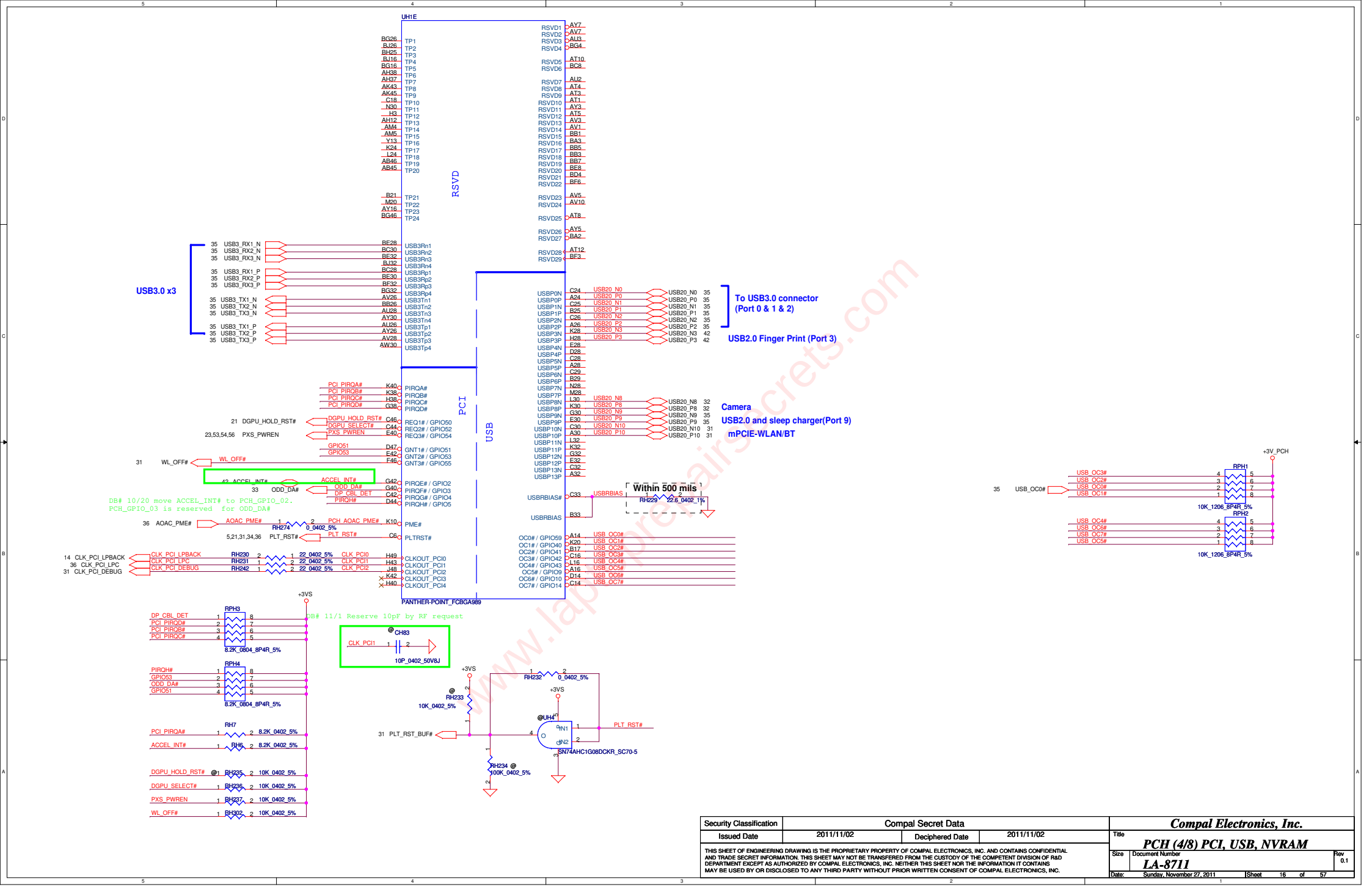

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **PCH (4/8) PCI, USB, NVRAM**

Size	Document Number	Rev
	LA-8711	0.1

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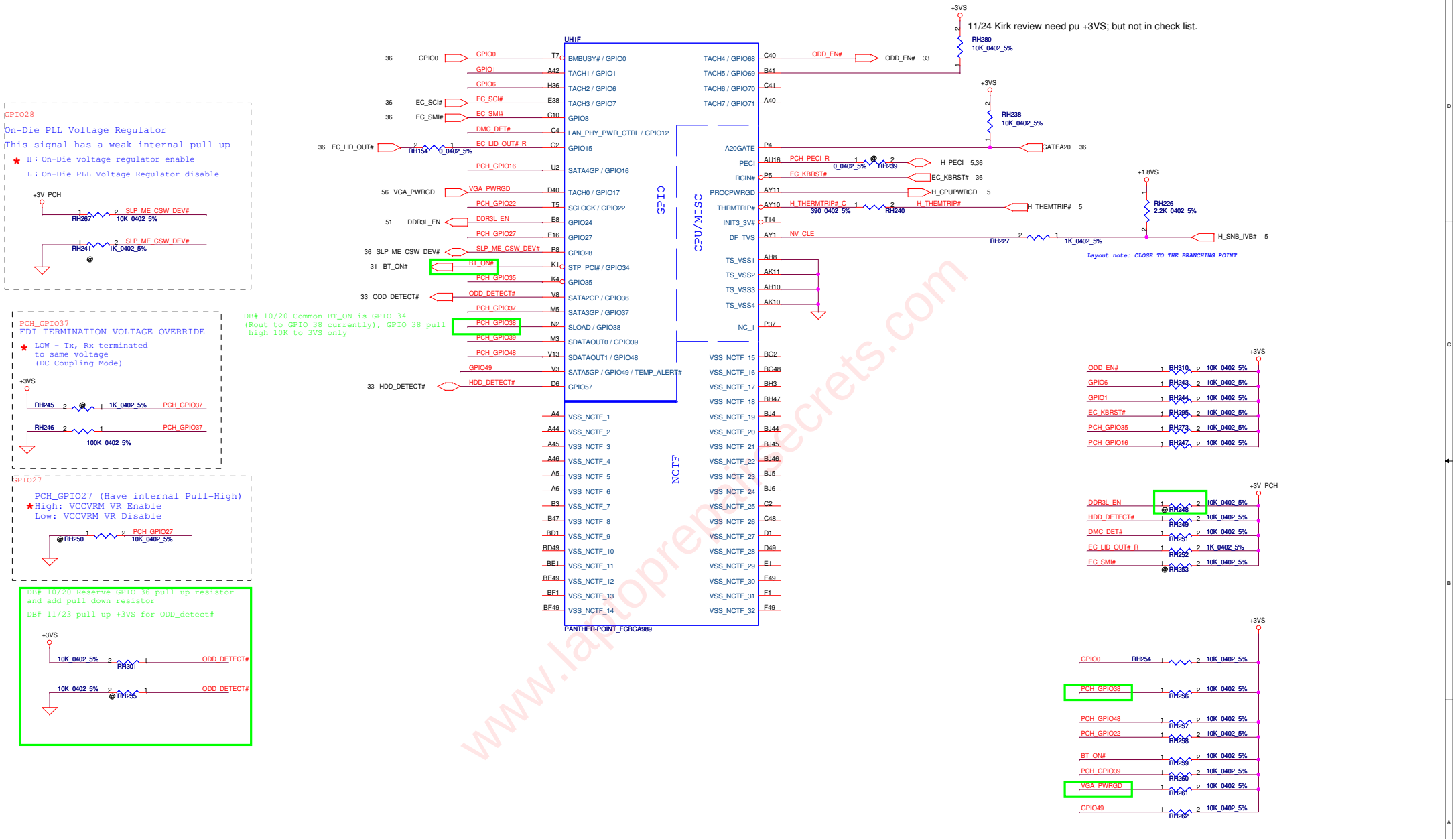

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: **PCH (5/8) GPIO, CPU, MISC**

Size	Document Number	Rev
	LA-8711	0.1

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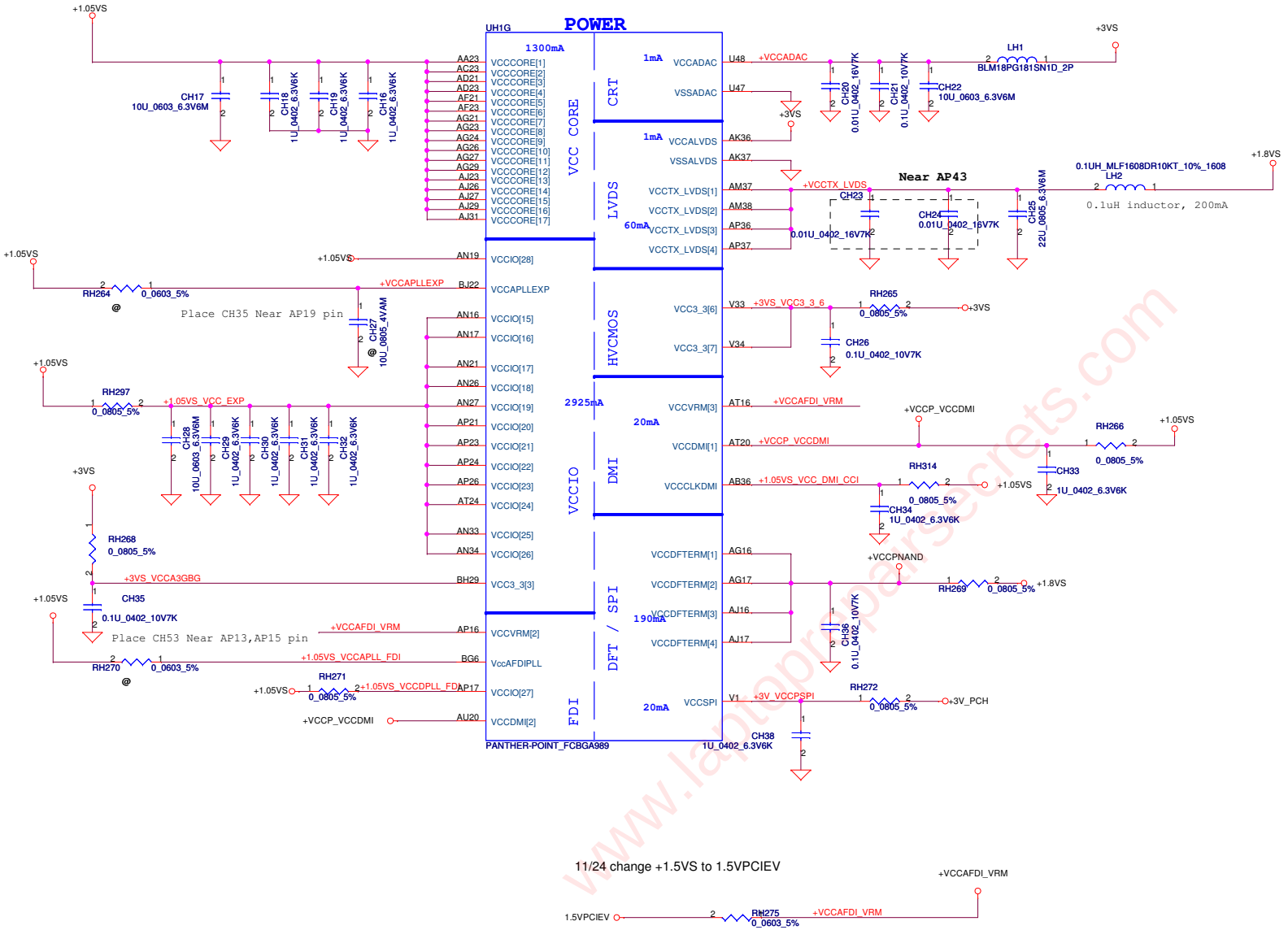


PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: **PCH (6/8) PWR**

Size: | Document Number: **LA-8711** | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 18 of 57

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

UH1J

PANTHER-POINT_FCBGA989

Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
MISC

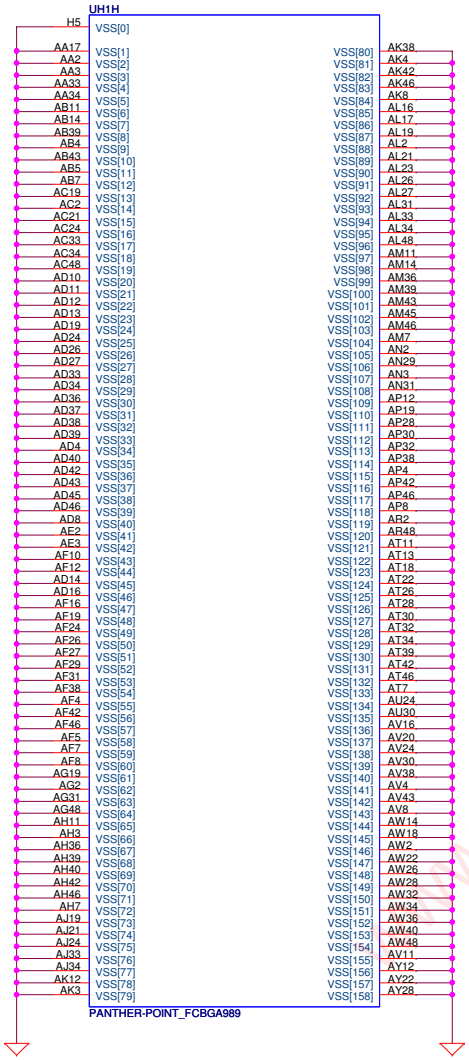
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

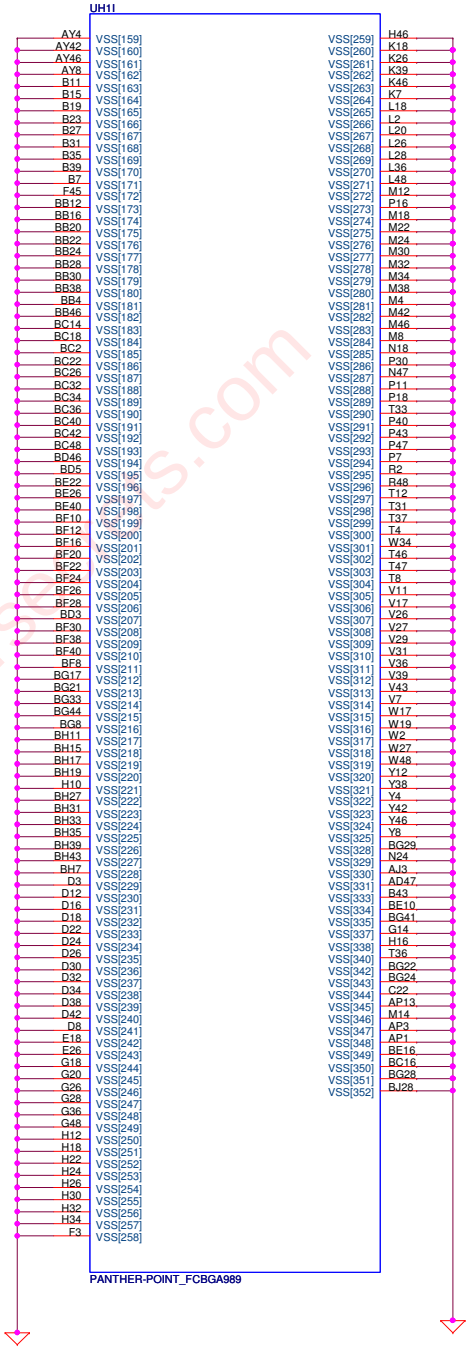
Compal Electronics, Inc.

Title: PCH (7/8) PWR

Size: | Document Number: LA-8711 | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 19 of 57





Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

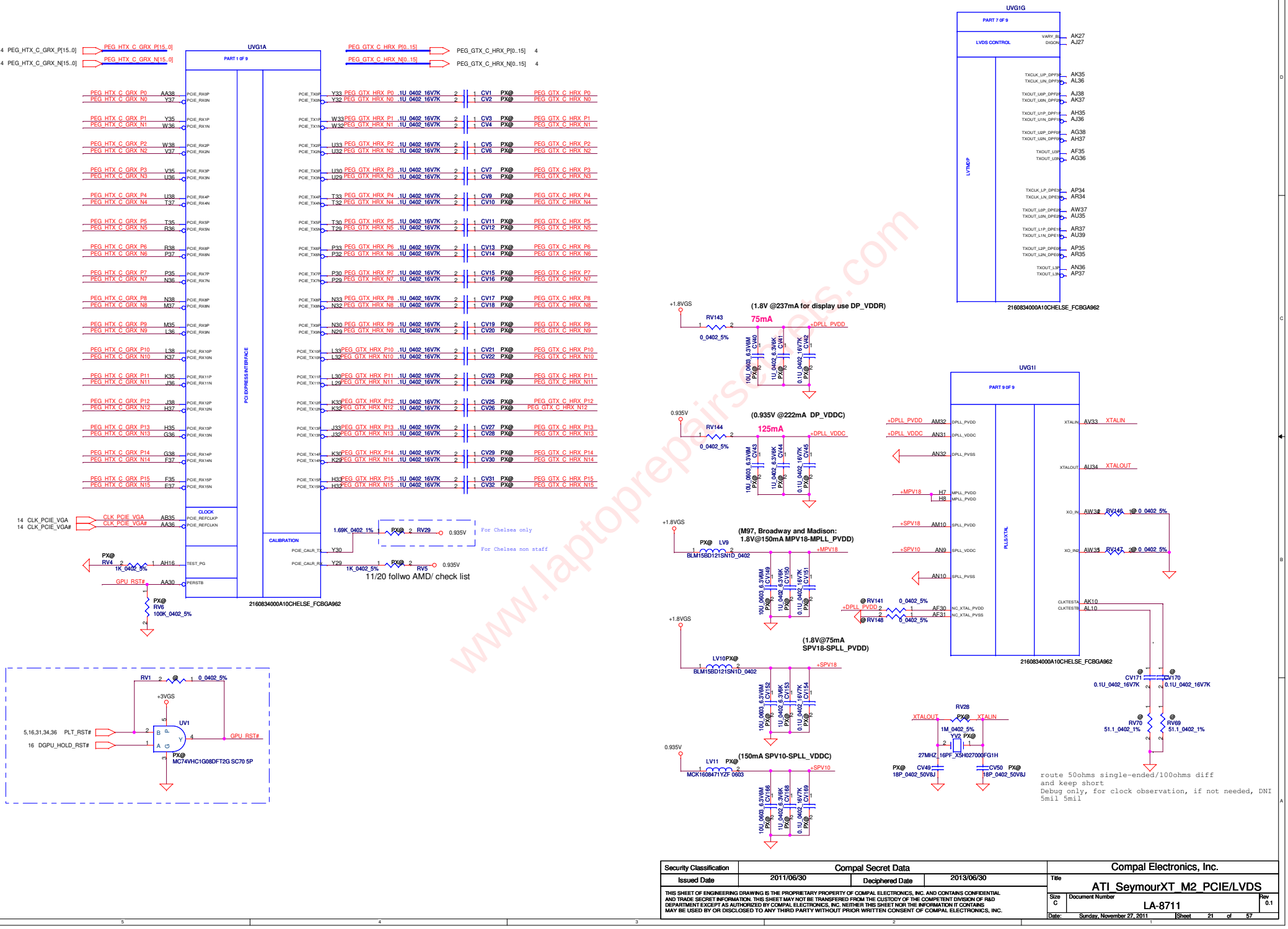
Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

Size	Document Number	Rev
	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 20 of 57

LVDS Interface



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.			
Title	ATI_SeymourXT_M2_PCIE/LVDS		
Size C	Document Number LA-8711		Rev 0.1
Date: Sunday, November 27, 2011		Sheet 21 of 57	

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS <all internal PD>	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE TRANSMITTER Power Saving Enable 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	Internal use only.This Pad has an internal PD and Must be 0V at reset. The pad may be left unconnected.	0
RSVD	H2SYNC		0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT GPIO13,12,11(config 2,1,0): internal PD. a)If BIOS_ROM_EN=1,the config[2:0] defines the ROM type. b)If BIOS_ROM_EN=0,the config[2:0] defines the primary aperture size Memory apertures config[3:0] 128MB 000 256MB 001 64MB 010	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defalit setting for desktop)

STRAPS

RV9 SMT-->@

Update net name

Internal VGA Thermal Sensor

Use Internal Thermal Sensor

External VGA Thermal Sensor: No stuff

UV1B — PART 2 OF 9

VRAM ID: VRAM_ID0, VRAM_ID1, VRAM_ID2

11/20 follow AMD/HP

0.60 V level, Please VREFG Divider ans cap close to ASIC

(1.8V@20mA TSVDD)

(1.8V@18mA AVDD)

(1.8V@117mA VDD1DI)

For Chelsea non staff

2160834000A10CHELSE_FCBGA962

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Main_MSIC

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 22 of 57

Name	FCH Pin Assignments
	Hudson-2 / Hudson-3
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192
PE_PWRGD	GPIO28

Chelsea Power Up

+3VGS/+VGA_CORE

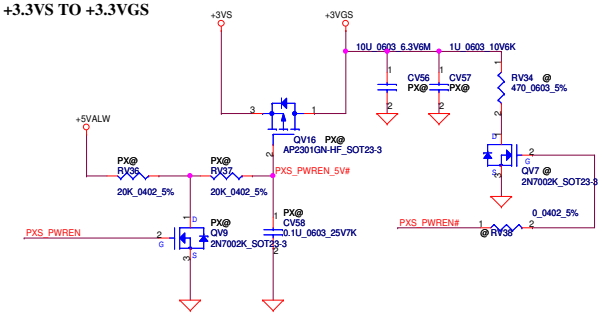
0,935V(VDDC)

VDDCI

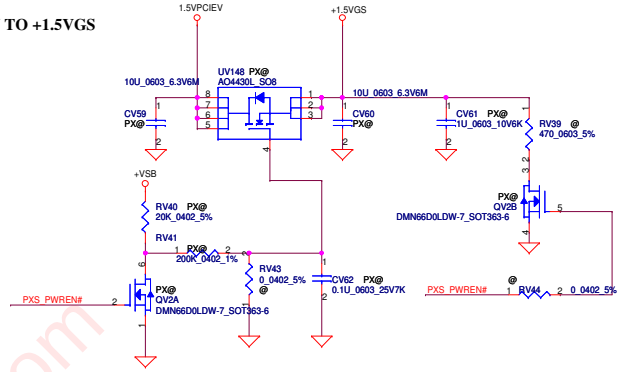
+1.5VGS(VDDR1/MVDDQ)

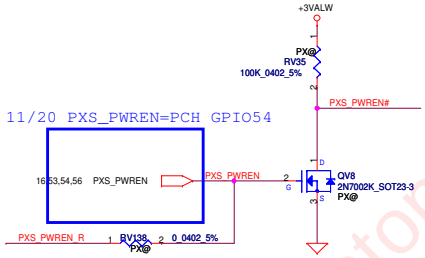
+1.8VS

+3.3VS TO +3.3VGS

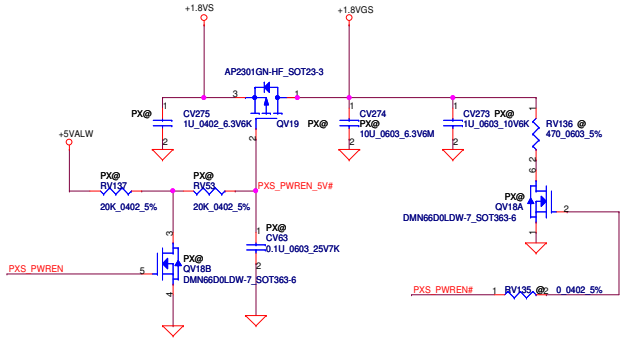


+1.5V TO +1.5VGS





+1.8VS TO +1.8VGS



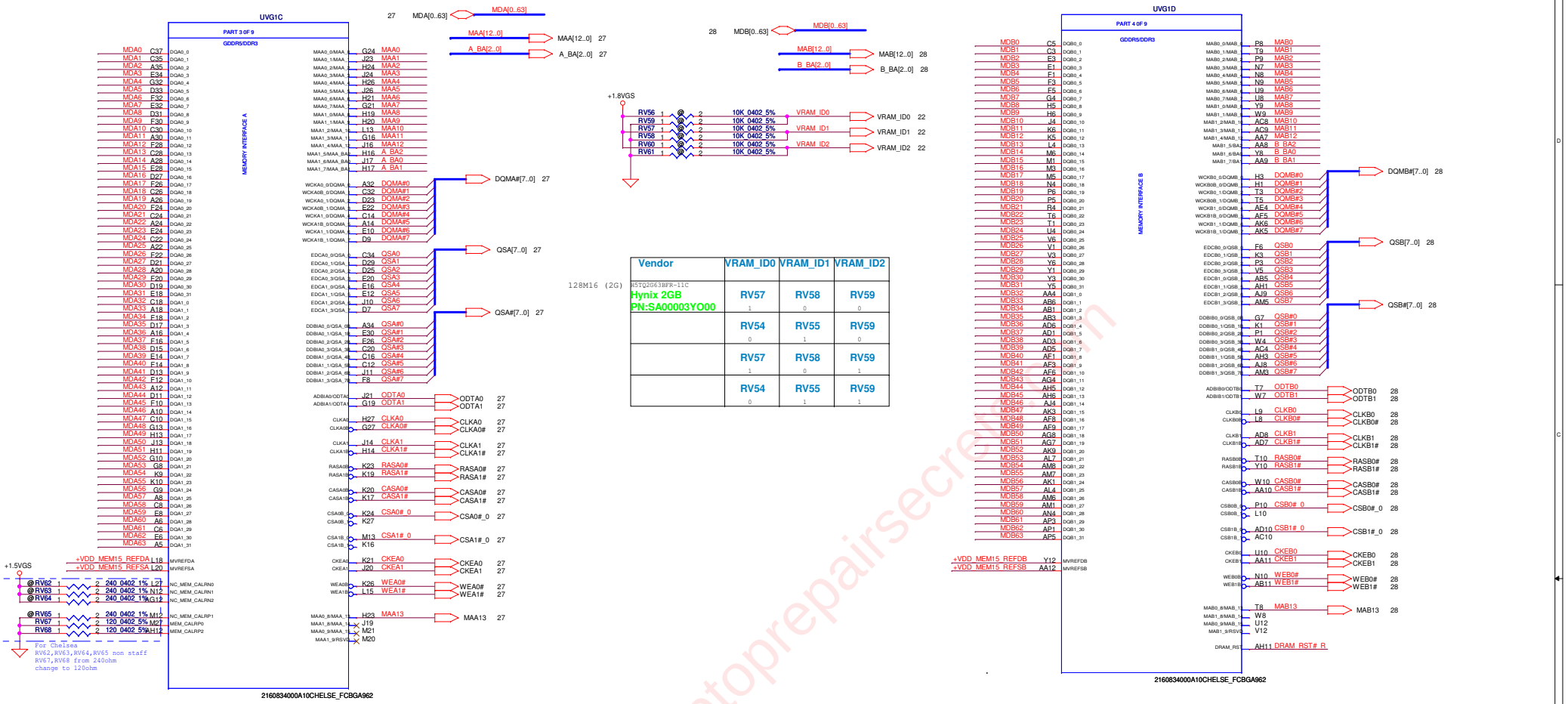
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_BACO POWER

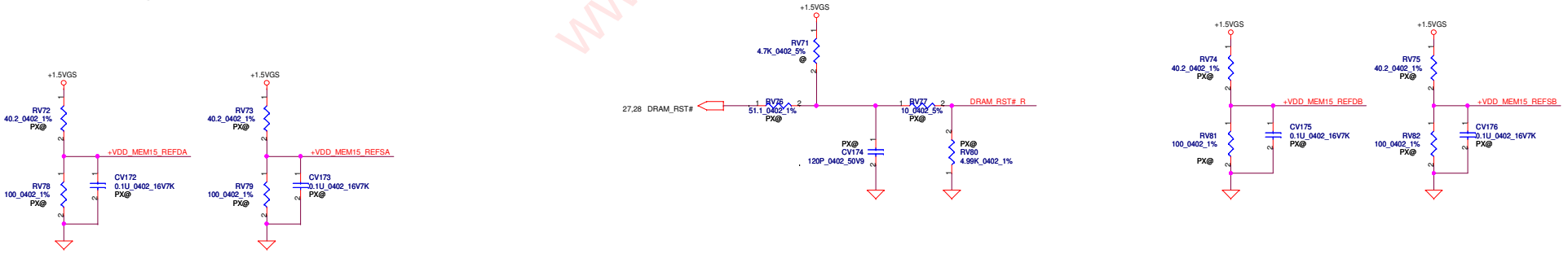
Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 Sheet 23 of 57



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
128M16 (2G) H5TQ2G63BFR-11C Hynix 2GB PN:SA00003YO00	RV57 1	RV58 0	RV59 0
	RV54 0	RV55 1	RV59 0
	RV57 1	RV58 0	RV59 1
	RV54 0	RV55 1	RV59 1

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



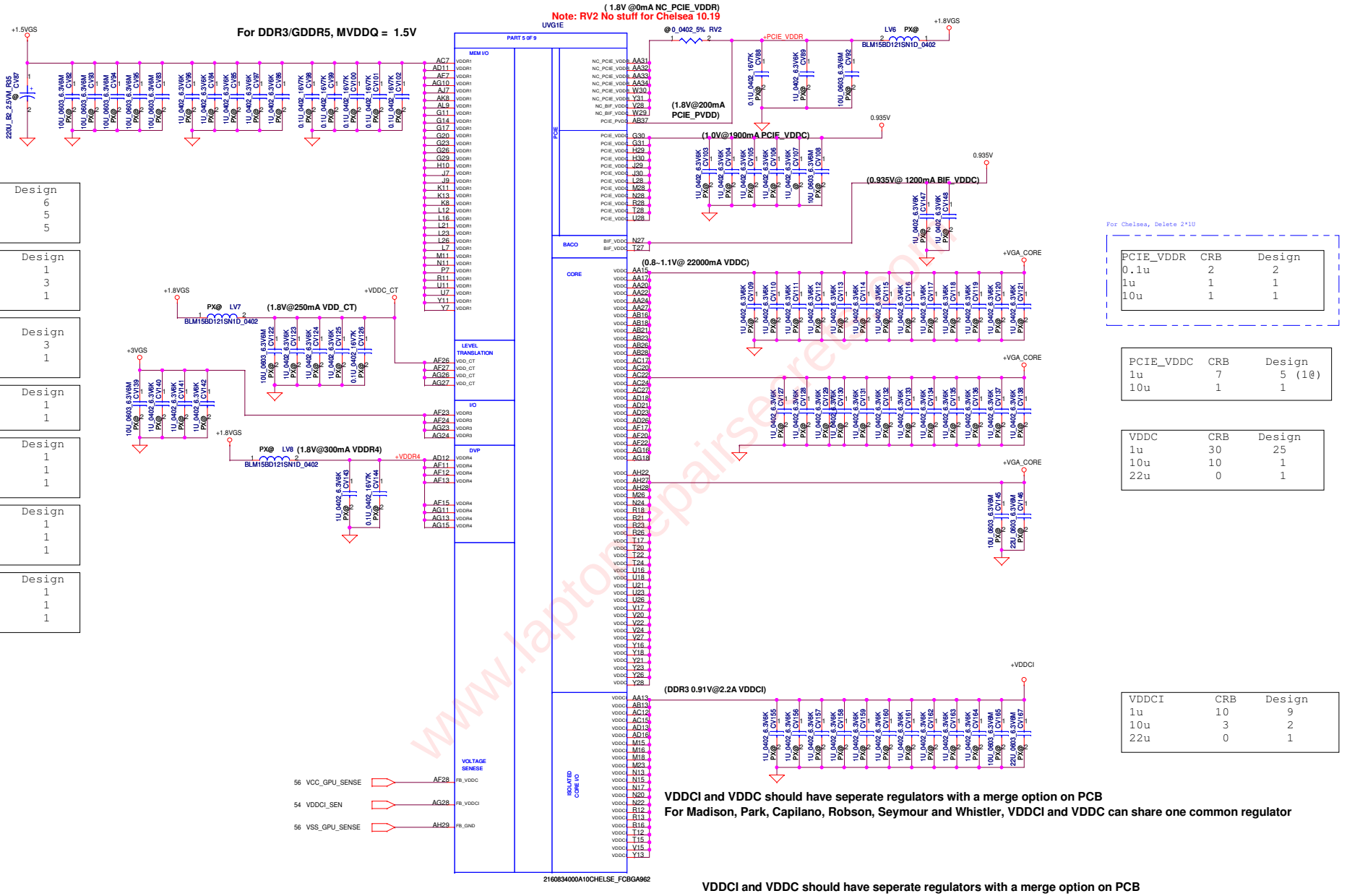
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_MEM IF

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 24 of 57



VDDR1	CRB	Design
0.1u	6	6
1u	10	5
10u	6	5

VDD_CT	CRB	Design
0.1u	1	1
1u	3	3
10u	1	1

VDDR3	CRB	Design
1u	3	3
10u	1	1

VDDR4	CRB	Design
0.1u	1	1
1u	1	1

MPV18	CRB	Design
0.1u	2	1
1u	2	1
10u	1	1

SPV18	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

SPV10	CRB	Design
0.1u	1	1
1u	1	1
10u	1	1

For Chelsea, Delete 2*1U

PCIE_VDDR	CRB	Design
0.1u	2	2
1u	1	1
10u	1	1

PCIE_VDDC	CRB	Design
1u	7	5 (1@)
10u	1	1

VDDC	CRB	Design
1u	30	25
10u	10	1
22u	0	1

VDDCI	CRB	Design
1u	10	9
10u	3	2
22u	0	1

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

VDDCI and VDDC should have seperate regulators with a merge option on PCB
For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

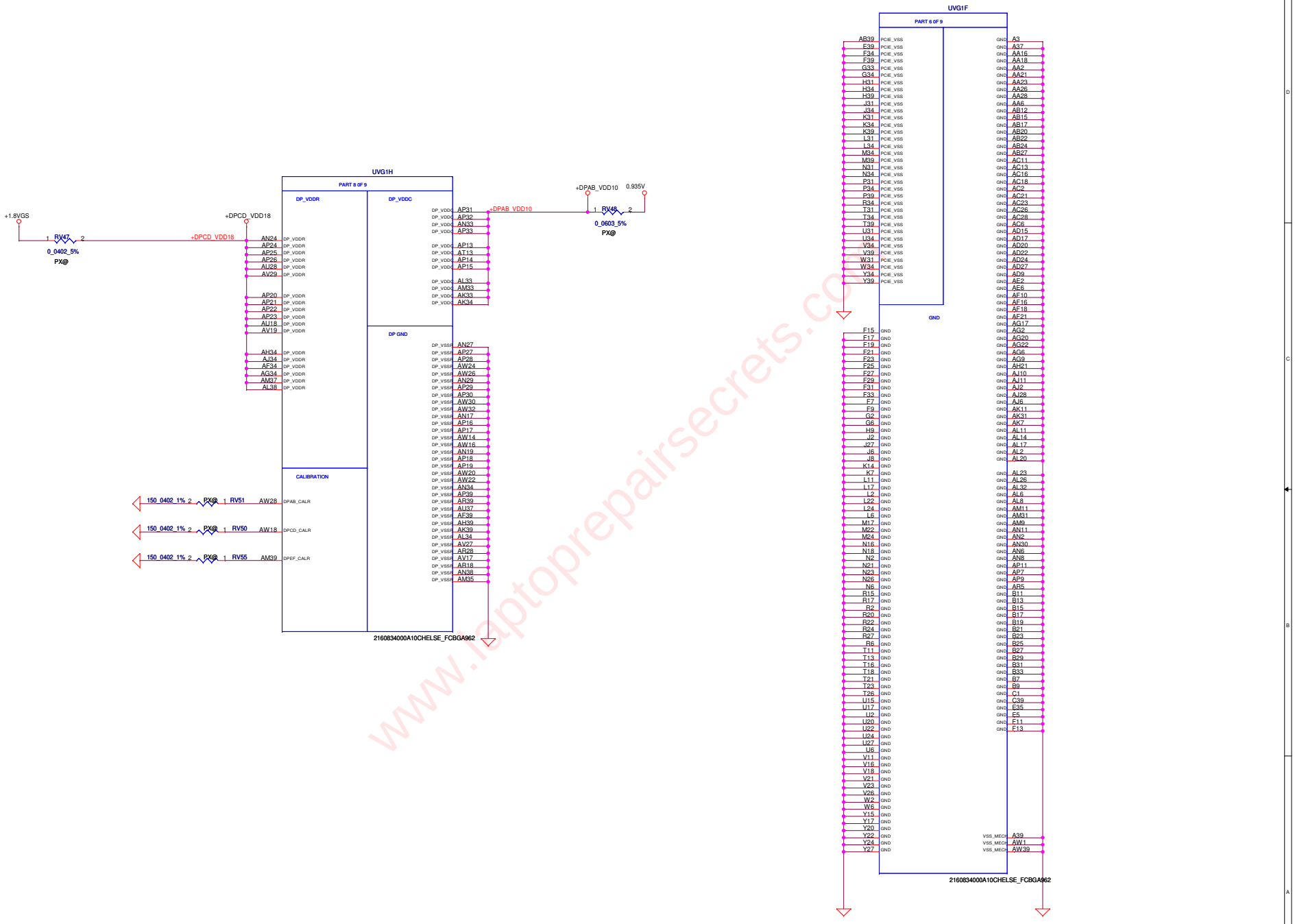
Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_Power

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 Sheet 25 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2013/06/30

Compal Electronics, Inc.	
Title	ATI_SetmourXT_M2_PWR_GND
Size: C	Document Number: LA-8711
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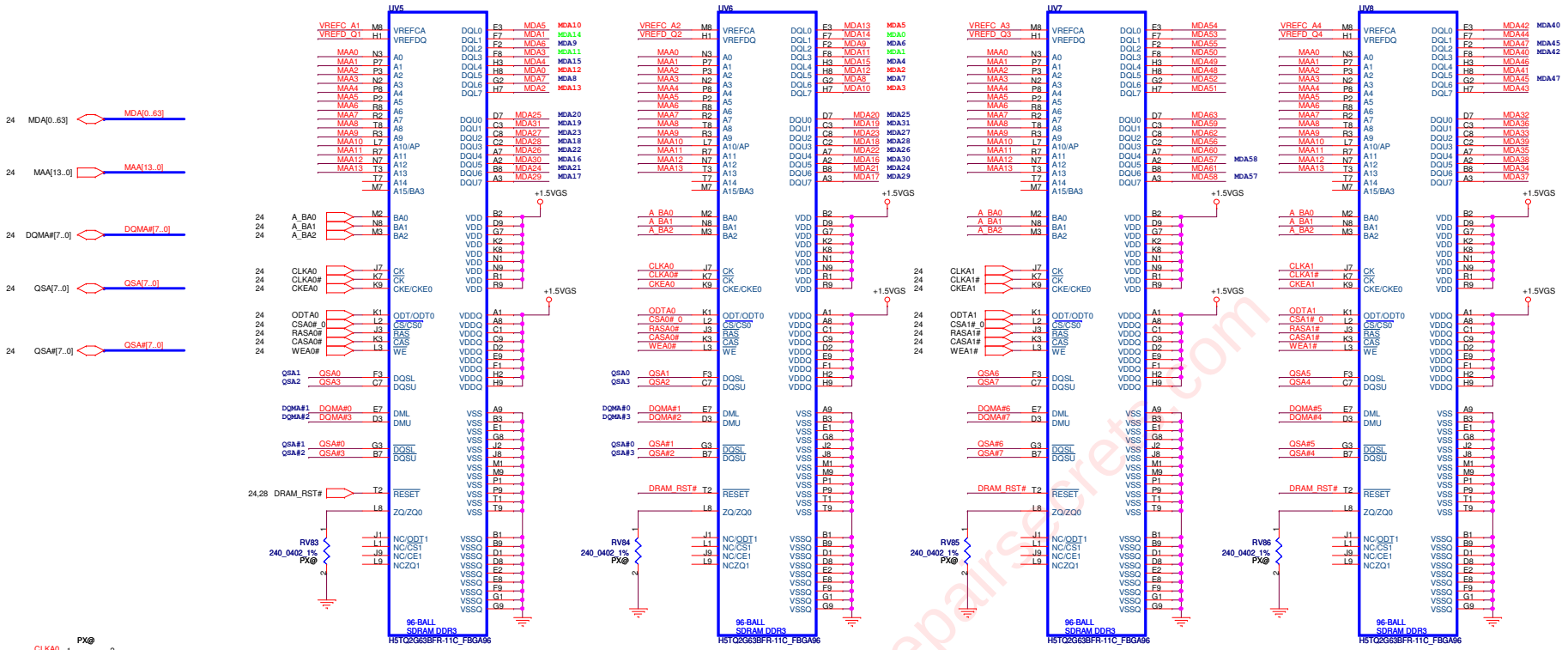
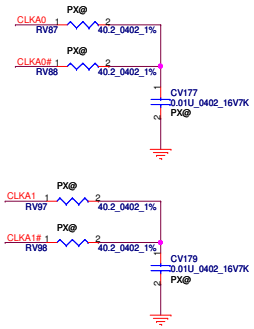
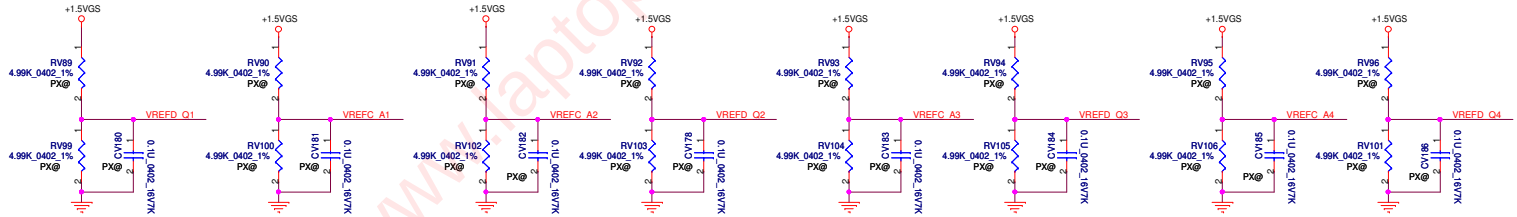
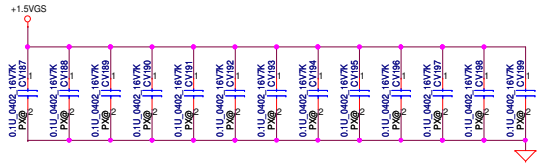
Date: Sunday, November 27, 2011	Sheet 26 of 57

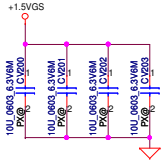
11/25 swap UV5.F8/ UV5.H8 =>MDA3/MDA0

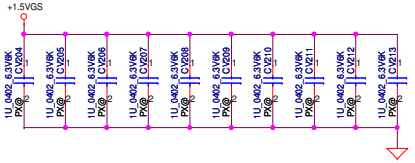


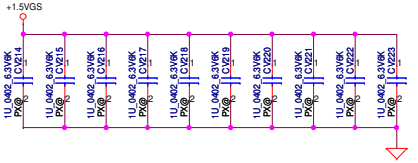












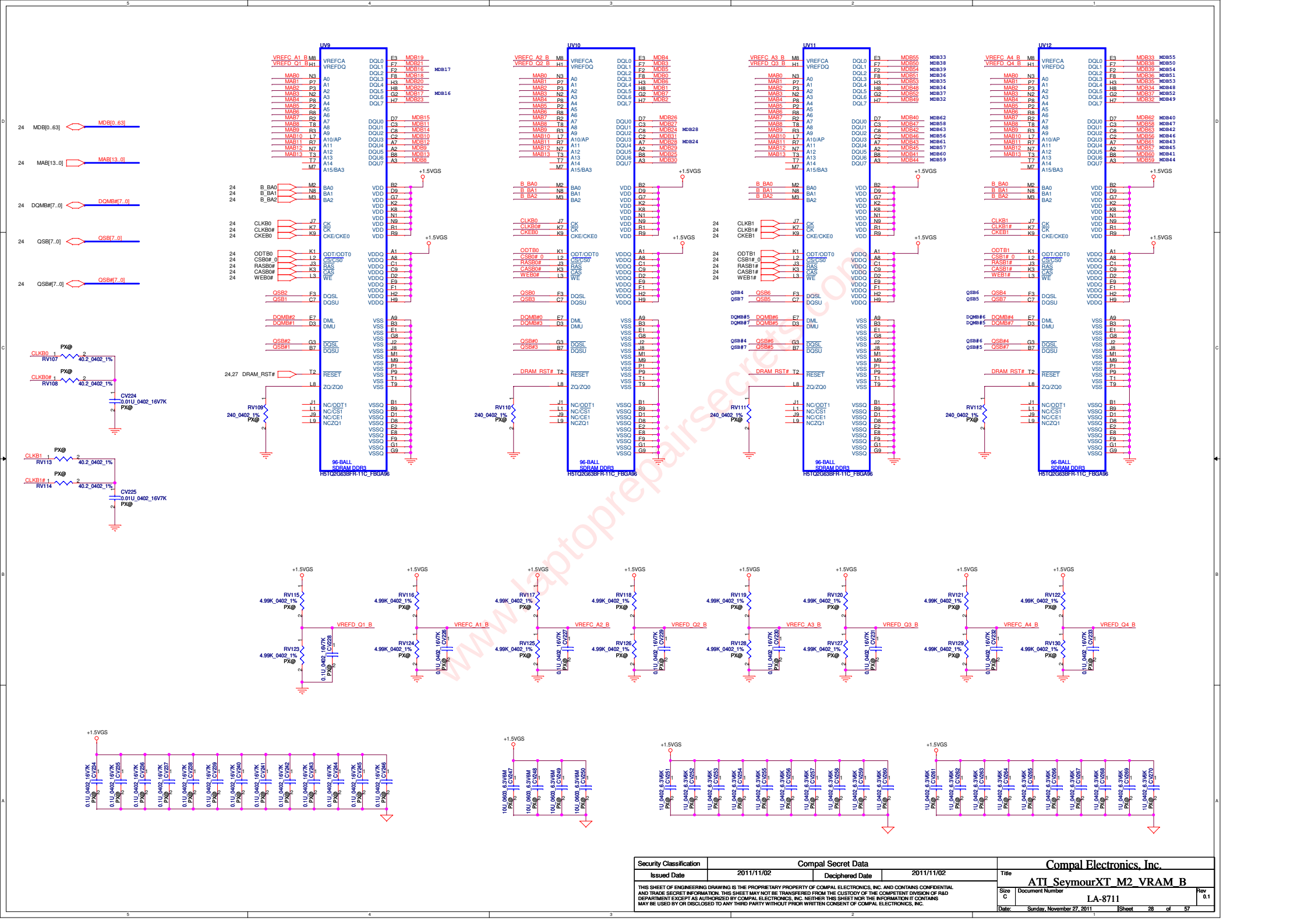
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_A

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 27 of 57



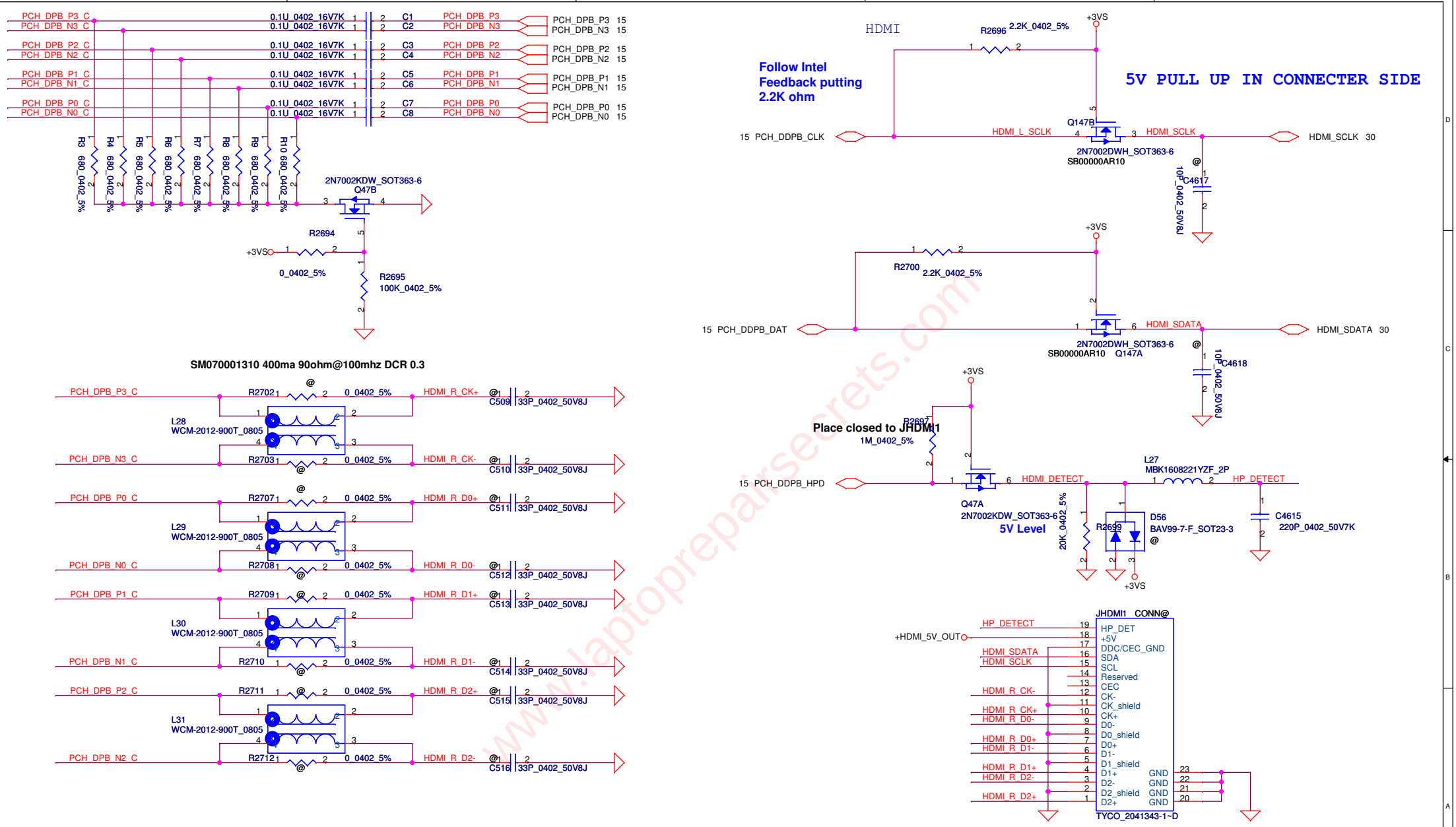
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: ATI_SeymourXT_M2_VRAM_B

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 28 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: **HDMI Conn**

Size	Document Number	Rev
	LA-8711	0.1

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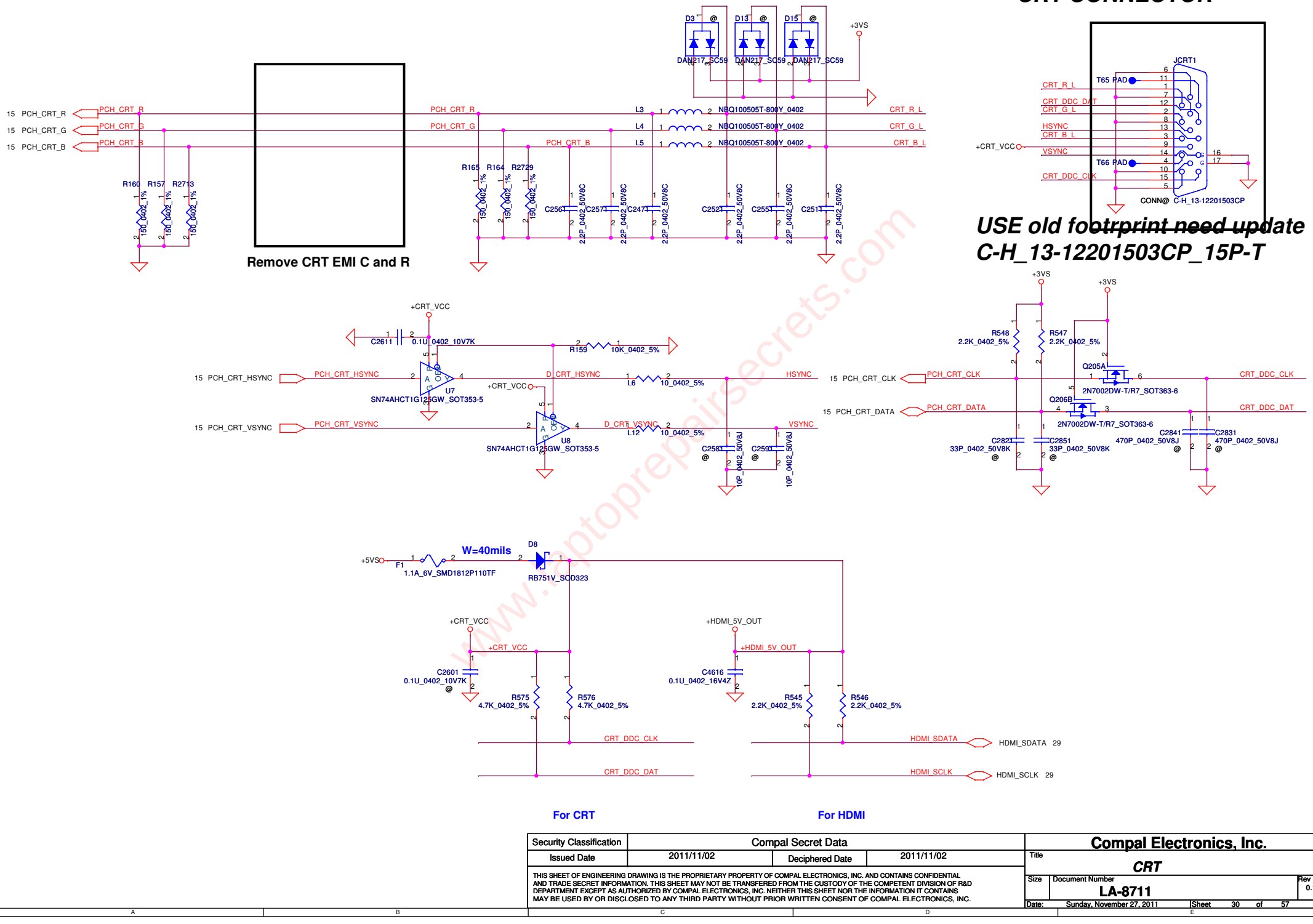
CRT CONNECTOR



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: **CRT**

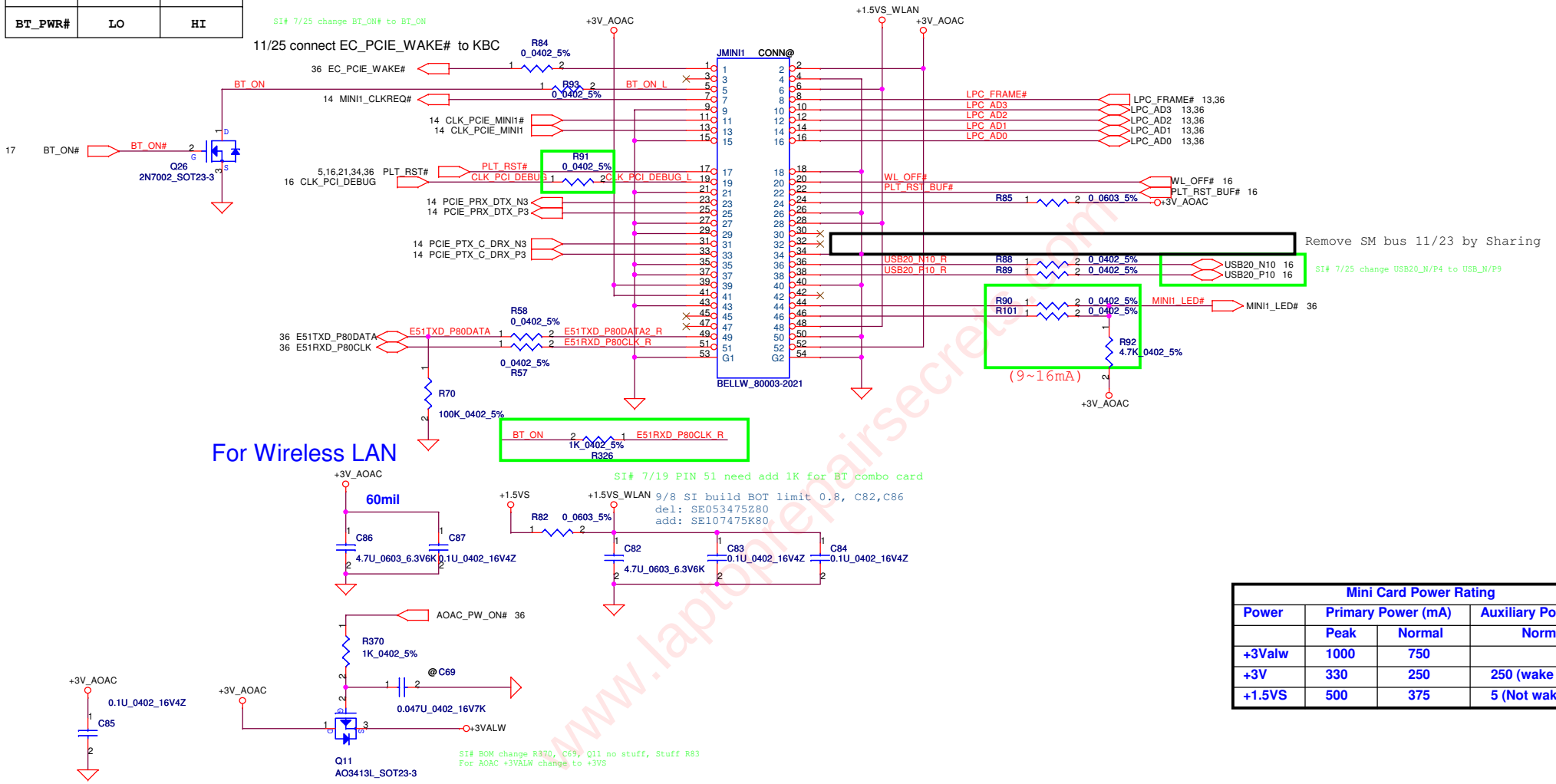
Size | Document Number: **LA-8711** | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 30 of 57

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	HI	LO
BT_PWR#	LO	HI

WLAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3Valw	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.			
Title: MiniCard & WLan			
Size	Document Number: LA-8711		Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 31 of 57		

SI# 8/15 R62 change to +3VALW, R61change to 10 ohm, R63 change to 200K ohm

LCD POWER CIRCUIT

+LCDVDD
R61 30_0603_5%
+3VALW
R62 100K_0402_5%
R63 200K_0402_5%
0.1U_0402_16V7K
C55
+3VS
W=60mils
Q7 AO3413L_SOT23-3
Q6A DMN66D0LDW-7_SOT363-6
0.01U_0402_25V7K C61
+LCDVDD
W=60mils
C63 0.1U_0402_16V4Z
C62 4.7U_0603_6.3V6K
15 PCH_ENVDD
PCH_ENVDD
Q6B DMN66D0LDW-7_SOT363-6

9/8 SI build BOT limit 0.8, C62
del: SE053475Z80
add: SE107475K80

Place closed to JLVDS1
+3VS
C56 0.1U_0402_16V4Z
+LCDVDD
C57 10U_0603_6.3V6M
C58 0.1U_0402_16V4Z

INVPWR_B+
W=60mils
L7 FBMA-L11-201209-221LMA30T_0805
L8 FBMA-L11-201209-221LMA30T_0805
B+
C59 680P_0402_50V7K
C60 68P_0402_50V8J
SM010014520 3000ma
220ohm@100mhz
DCR 0.04

LCD/LED PANEL Conn.

W=60mils W=60mils

+3VS
R64 2.2K_0402_5% LCD_CLK
R65 2.2K_0402_5% LCD_DATA
@C64 10P_0402_50V8J
@C65 10P_0402_50V8J
C66 220P_0402_50V7K INVTPWM
C67 220P_0402_50V7K DISPOFF#

Check pin definition.

11/23 remove INVT_PWM

15 DPST_PWM
R197 0_0402_5%
INVTPWM
@ R72 10K_0402_5%

36 BKOFF#
BKOFF# R76 33_0402_5% DISPOFF#
R74 10K_0402_5%

15 PCH_LCD_CLK
PCH_LCD_CLK R193 0_0402_5% LCD_CLK
15 PCH_LCD_DATA
R194 0_0402_5% LCD_DATA

16 USB20_P8
16 USB20_N8
@ R156 0_0402_5%
L11
USB20_P8_R
USB20_N8_R
WCM-2012-900T_4P
R229 0_0402_5%
@
8/19 change stuff L26 by EMI request

D55
D_MIC_CLK
D_MIC_DATA
PESD5V0U2BT
@
6/27 Add ESD solution

+LCDVDD
JLVDS1
LCD_CLK
LCD_DATA
15 PCH_TXOUT0+
15 PCH_TXOUT0-
15 PCH_TXOUT1+
15 PCH_TXOUT1-
15 PCH_TXOUT2+
15 PCH_TXOUT2-
15 PCH_TXCLK+
15 PCH_TXCLK-
USB20_N8_R
USB20_P8_R
DISPOFF#
INVTPWM
INVPWR_B+
+3VS
D_MIC_CLK
D_MIC_DATA
GND
STARC_111H30-000000-G4-R
CONN@

38 D_MIC_CLK_L_C
38 D_MIC_DATA_C
D_MIC_CLK_L_C
D_MIC_DATA_C
100_0402_5%
RA13
D_MIC_CLK_L
LA19 FBMA-L10-160808-301LMT_2P
D_MIC_CLK
D_MIC_DATA
LA20 FBMA-L10-160808-301LMT_2P

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

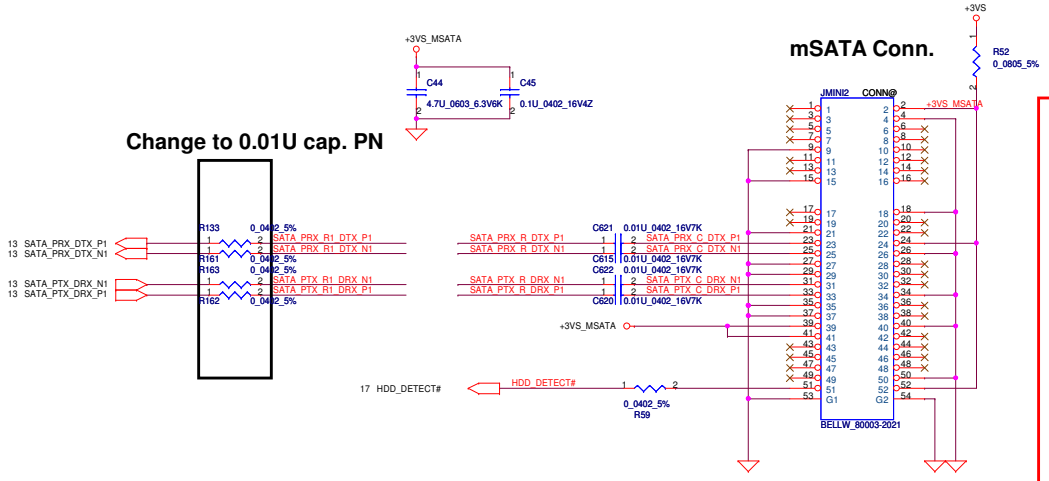
Title: **LVDS Connector**

Size	Document Number	Rev
	LA-8711	0.1

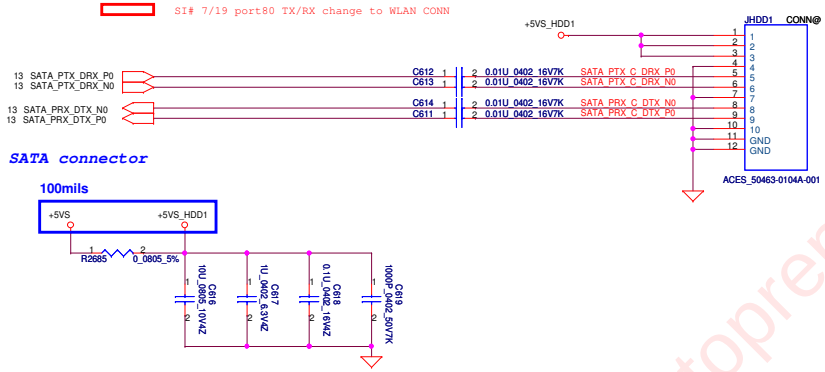
Date: Sunday, November 27, 2011 Sheet 32 of 57

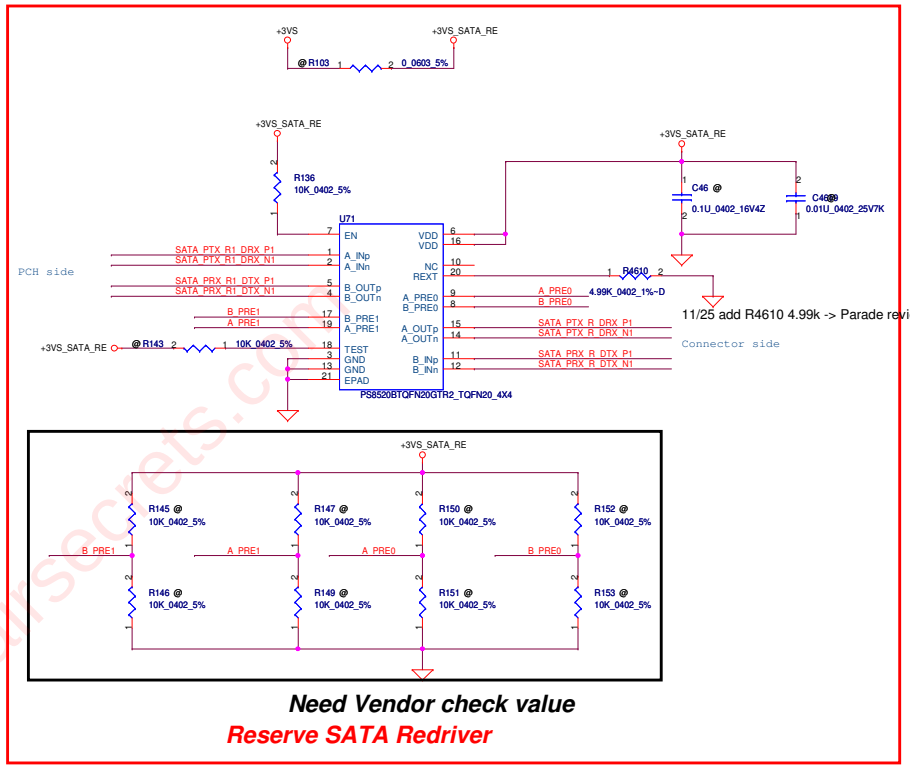
PV# 9/17 JMINI2/JMINI3 change footprint follow ME connector list

mSATA Conn.

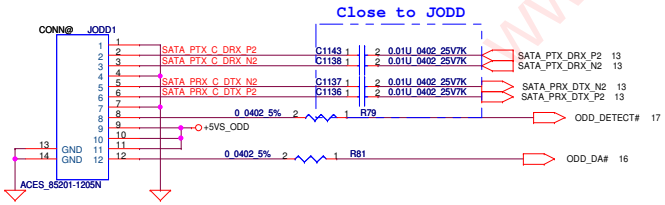


SI# 7/19 port80 TX/RX change to WLAN CONN

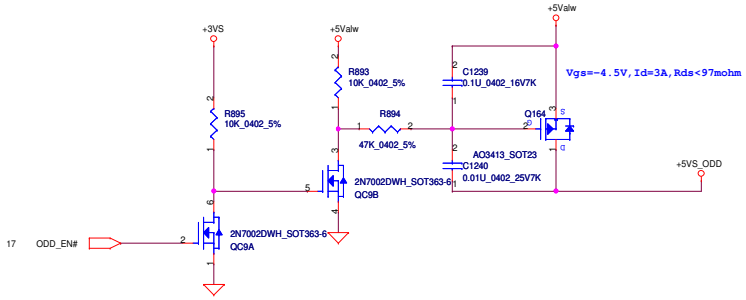




SATA ODD Conn



Place components closely ODD CONN.
11/24 remove 22uF to sub board



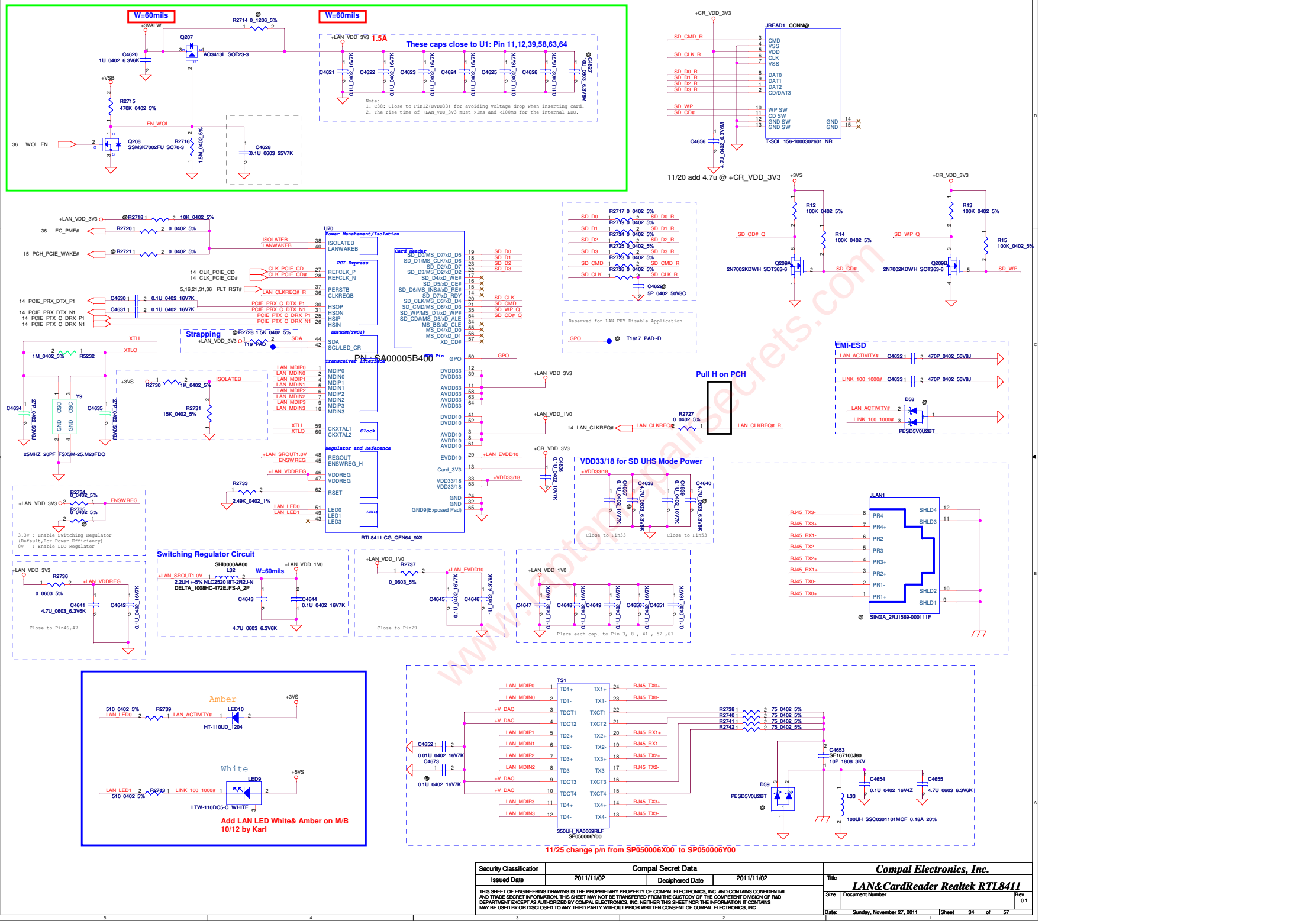
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: mSATA Connector

Size	Document Number	Rev
C	LA-8711	0.1

Date: Sunday, November 27, 2011 | Sheet 33 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

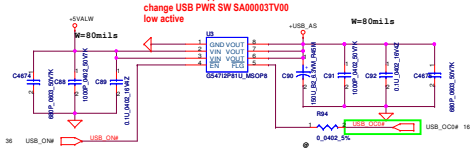
Title: **LAN&CardReader Realtek RTL8411**

Size	Document Number	Rev
		0.1

Date: Sunday, November 27, 2011 Sheet 34 of 57

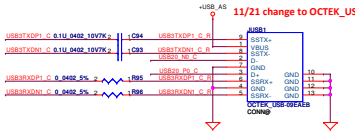
USB3.0

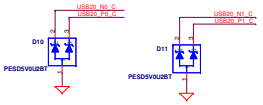
USB3.0 need support 2.5A
change USB PWR SW SA00003TV00
low active

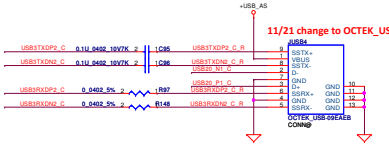


SI# 8/8 change USB_OC0# to USB30_OC#

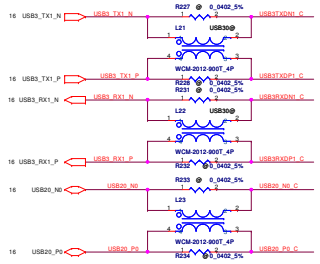
11/21 change to OCTEK_USB-09EAEB

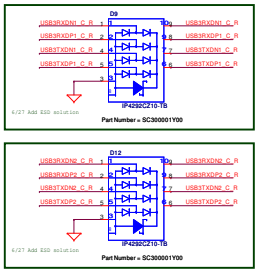


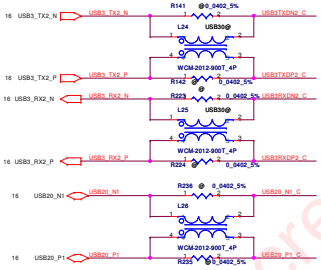




11/21 change to OCTEK_USB-09EAEB

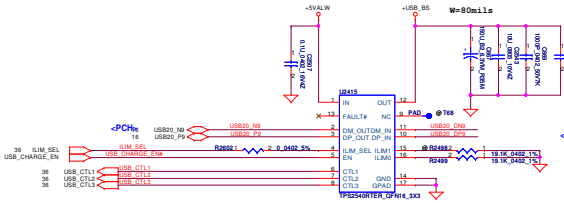


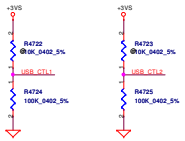




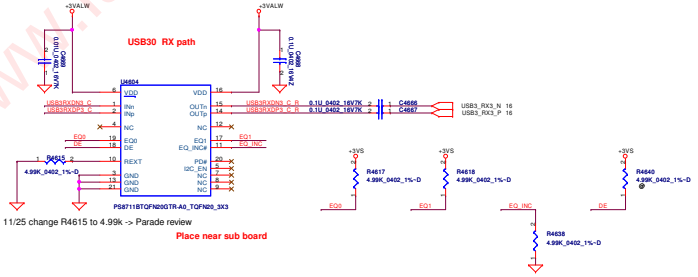
USB2.0 charger

USB charger footprint need change to TPS2543





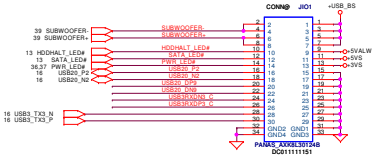
State	S0				S3, S4, S5			
Mode	CDP				DCP			
Control pin	CTL1	CTL2	CTL3	ILIM_SEL	CTL1	CTL2	CTL3	ILIM_SEL
	1	1	X	1	0	0	1	1



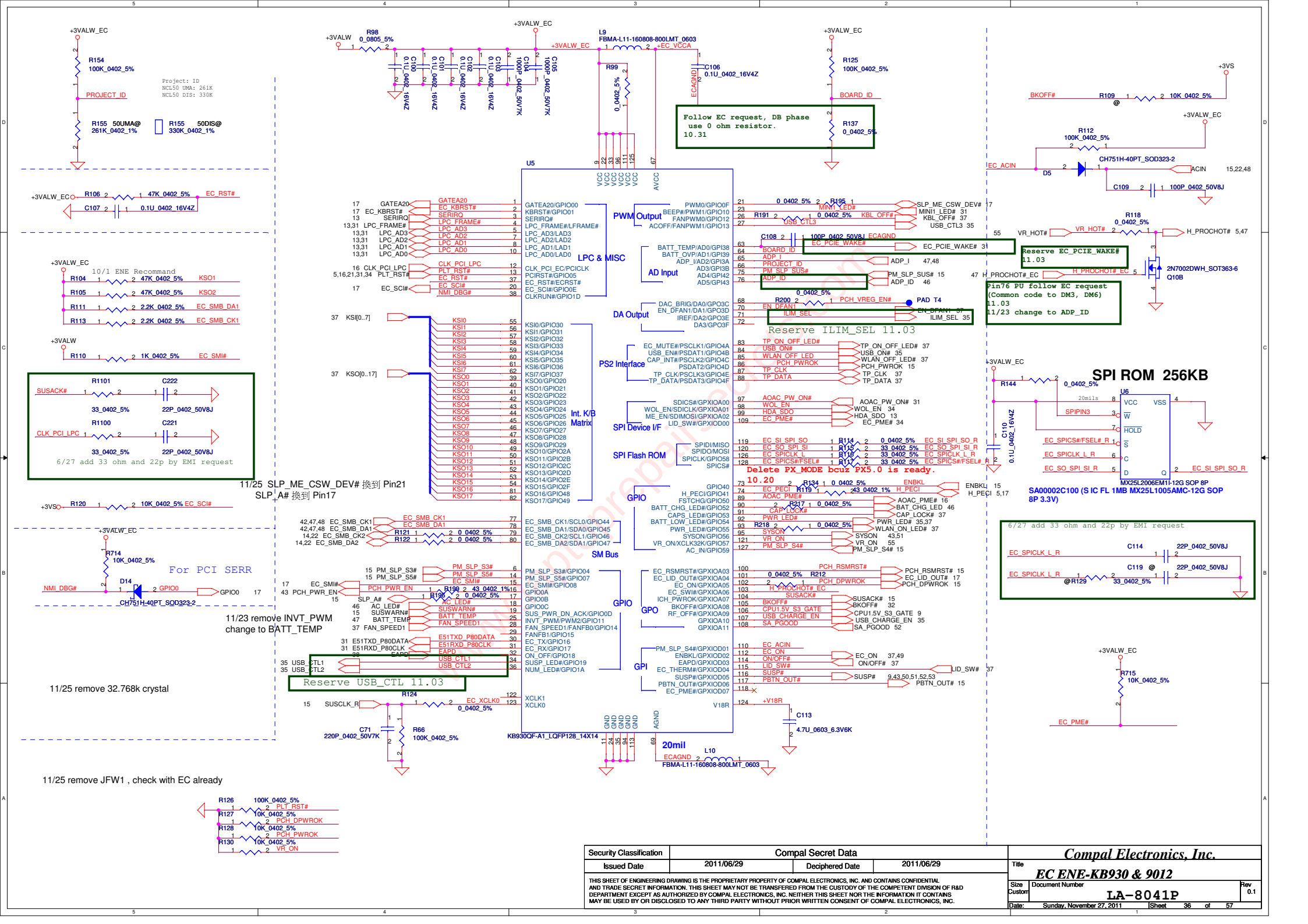
11/25 change R4615 to 4.99k -> Parade review

Place near sub board

11/21 follow AMD change to 30 pin



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/02	Deciphered Date	2011/11/02
Title	USB Con & Daughter Con		
Size D	Document Number LA-8041P		Rev 0.1
Date: Sunday, November 27, 2011	Sheet 35 of 57		



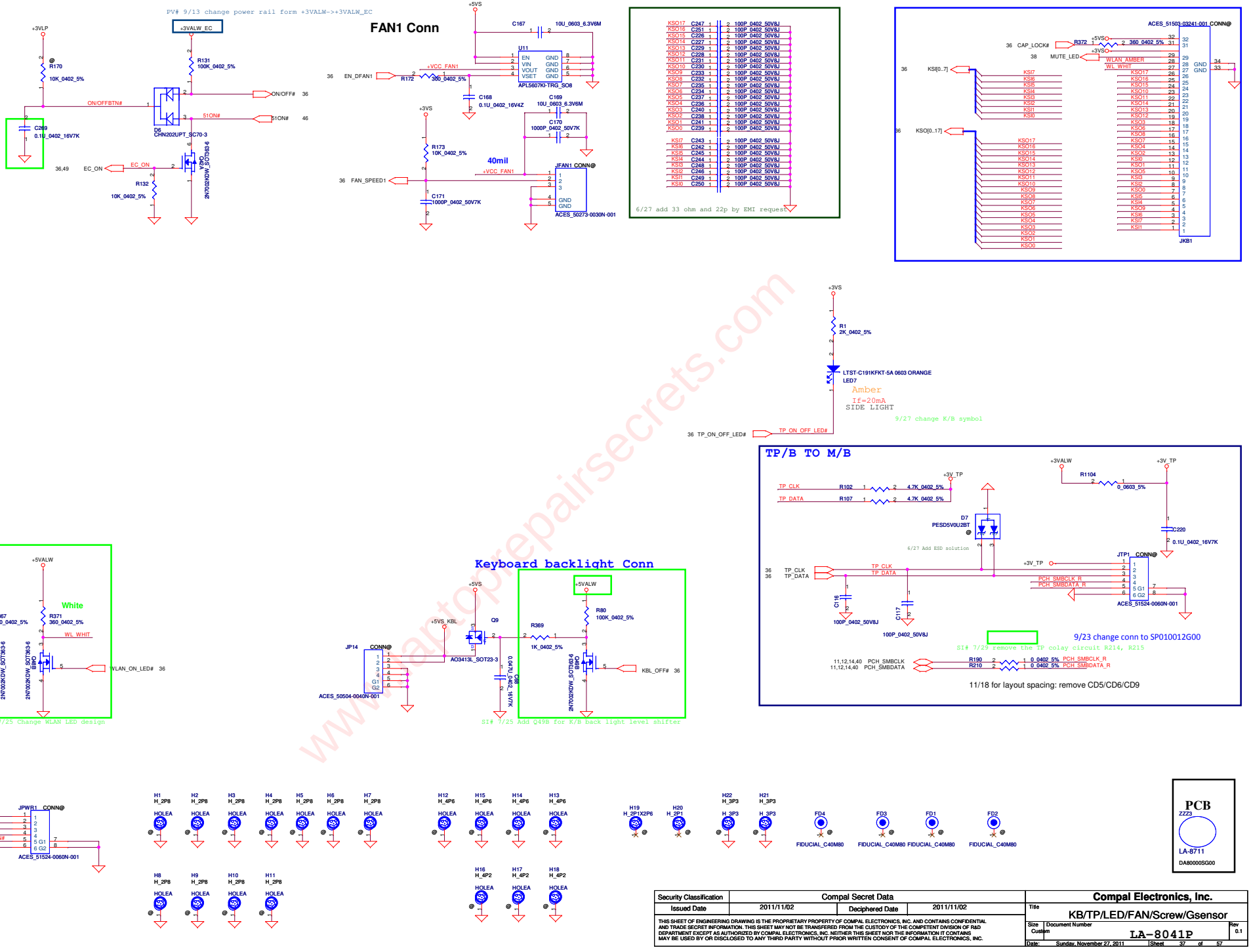
Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.

Title: EC ENE-KB930 & 9012

Size	Document Number	Rev
Custom	LA-8041P	0.1

Date: Sunday, November 27, 2011 Sheet 36 of 57



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: KB/TP/LED/FAN/Screw/Gsensor

Size	Document Number	Rev
Custom	LA-8041P	0.1

Date: Sunday, November 27, 2011 | Sheet 37 of 57

DVDD_IO should match
with HDA Bus level(optional for 3.3V signaling or 1.5V signaling)

Place AVDD ,PVDD,and DVDD capacitor close to Codec

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

PLACE CLOSE TO U1 PIN 13

If Sense_A total length is greater than 6 inches, chagne C12 to 0.1uF

RA9 2.49K_0402_1% +AVDD_CODEC
RA7 20K_0402_1% HP_JD HP_JD 41
SENSE_A CA1 1000P_0402_50V7K

SENSE_B RA10 10K_0402_1% +AVDD_CODEC 11/21 RA10 change to 10K(un-used)
CA11 1000P_0402_50V7K

If Sense_B is un-used, then pull high Sense_B to AVDD by 10Kohm resistor

PLACE CLOSE TO U1 PIN 14

UA5 92HD91B2X5NLGXYAX8_QFN48_7X7

DVDD_CORE, DVDD_IO, DVDD, HDA_BITCLK, HDA_SDO, HDA_SYNC, HDA_SDI, HDA_RST#, EAPD, DMIC_CLK/GPIO1 DMIC0/GPIO2, SPDIFOUT0/GPIO3 DMIC1/GPIO0/SPDIFOUT1, CAP+, CAP-, DVSS, PVSS, PAD

AVDD1 AVDD2, PVDD1 PVDD2, SENSE_A SENSE_B, HP0_PORTA_L HP0_PORTA_R VREFOUT_A, HP1_PORTB_L HP1_PORTB_R, PORTC_L PORTC_R VREFOUT_C/GPIO4, PORTE_L PORTE_R, PORTF_L PORTF_R, SPK_PORTD_+L SPK_PORTD_-L, SPK_PORTD_+R SPK_PORTD_-R, MONO_OUT, PCBEEP, VREFFILT CAP2 V- VREG(+2.5V), AVSS1 AVSS2 AVSS3

HP Jack
Ext MIC

Internal SPKR
(front stereo speaker)

Place C208 close to Codec

Place C209,C210,CA87,CA89 close to Codec

SB Beep

9/27 LDO TPS793475DBVR for audio power

UA2 TPS793475DBVR_SOT23-5 VIN EN VOUT BYPASS GND

GND GNDA

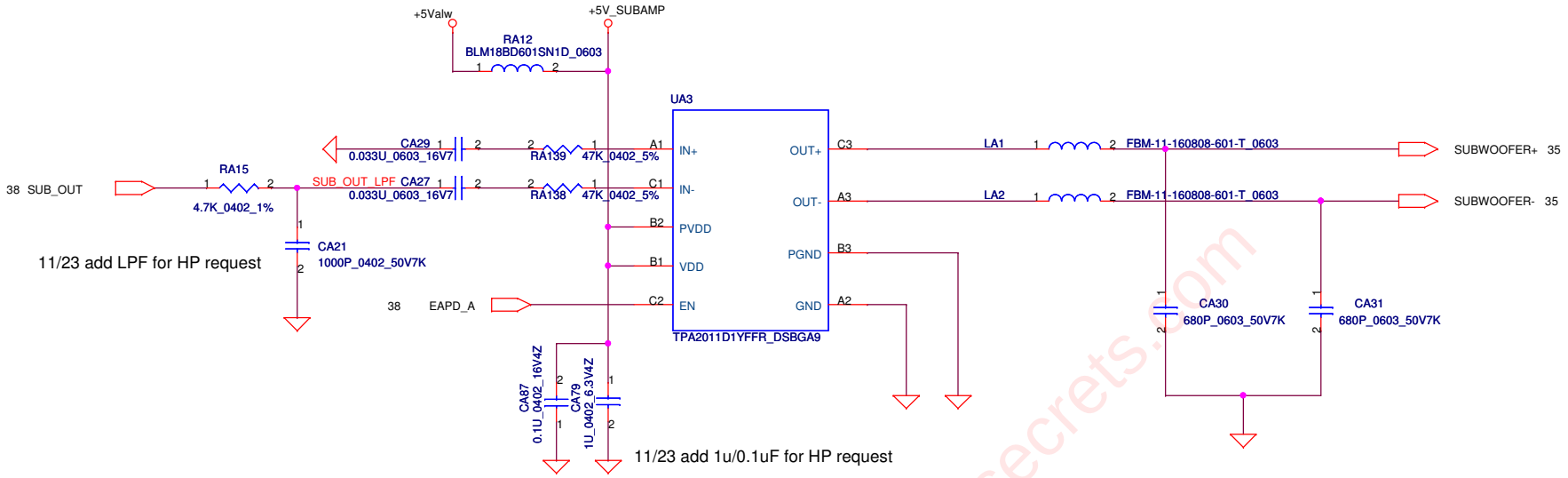
Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

Title: Audio IDT 92HD91

Size	Document Number	Rev
Custom		0.1

Date: Sunday, November 27, 2011 Sheet 38 of 57



2011.10.28 Change Sub-woofer Amp to TPA2011D1

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

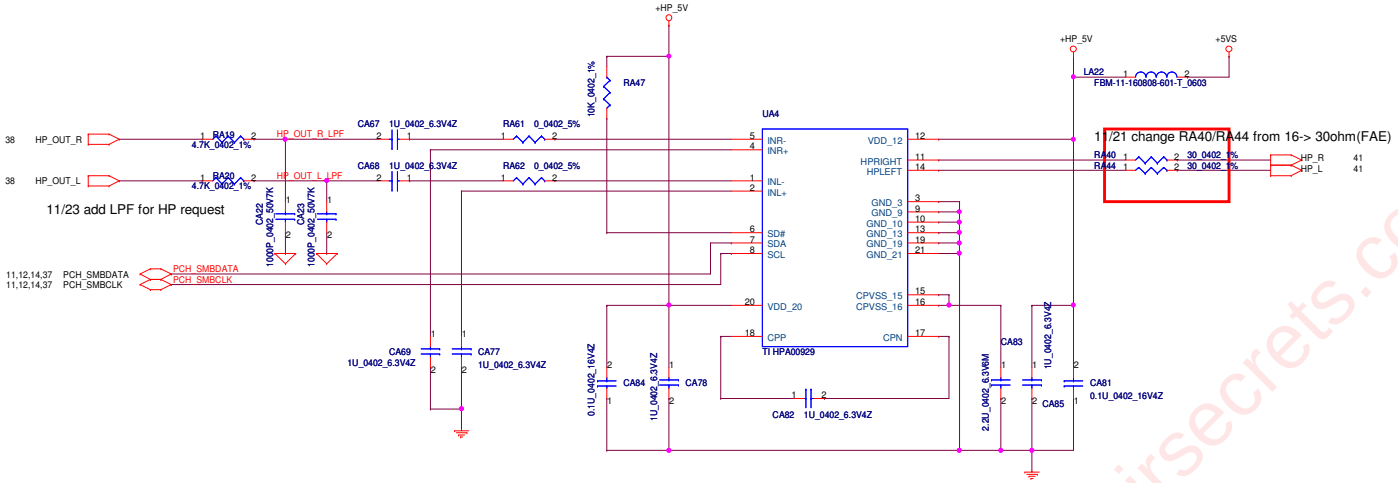
Compal Electronics, Inc.

Title: Audio Woofer Amplifier

Size	Document Number	Rev
B		0.1

Date: Sunday, November 27, 2011 Sheet 39 of 57

Headphone Amp

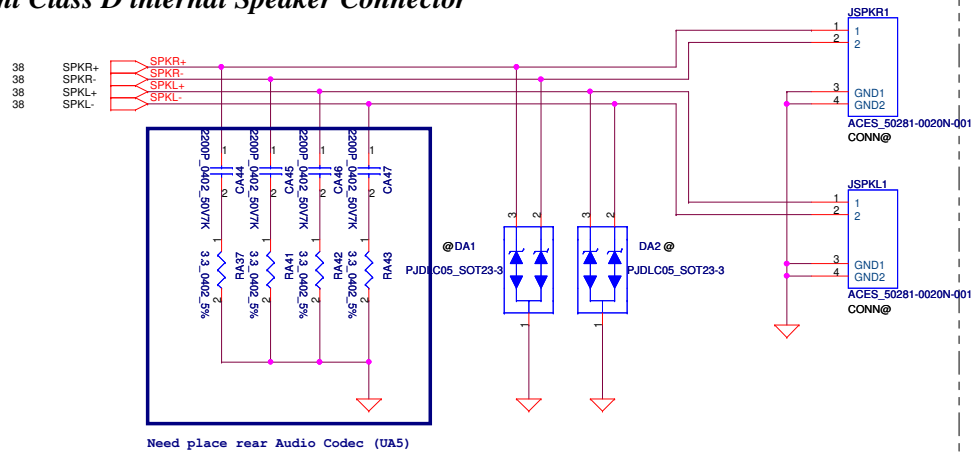


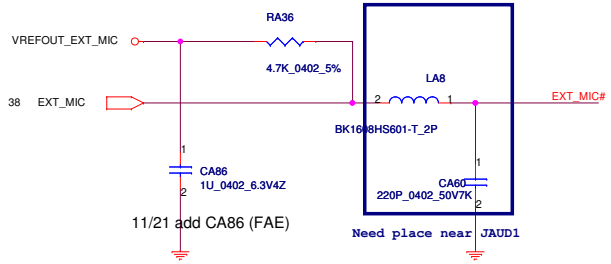
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/02	Deciphered Date 2011/11/02	Title: Audio SPK/HP Amplifier

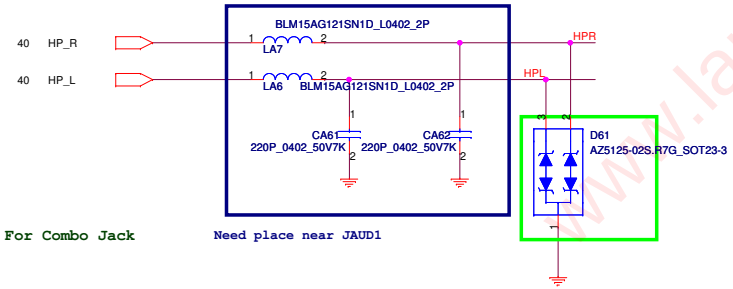
Size: Custom	Document Number		Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 40 of 57		

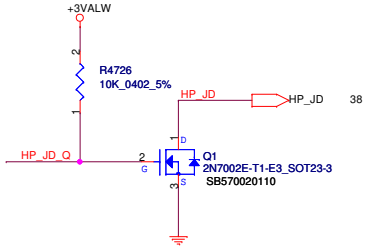
Front Class D internal Speaker Connector

11/25 change SPKR connector follw AMD

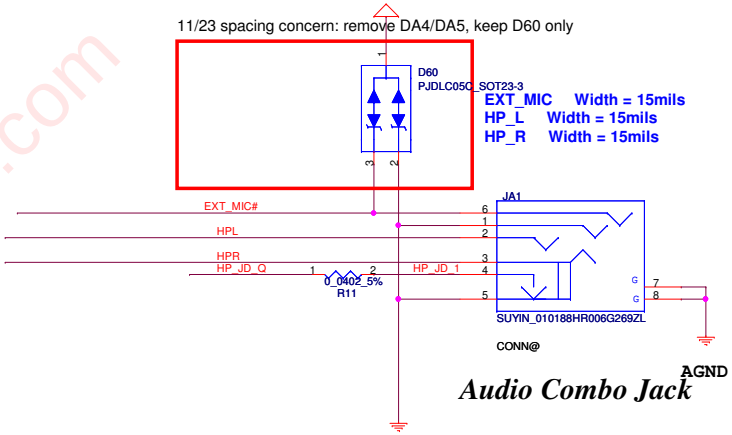








11/23 spacing concern: remove DA4/DA5, keep D60 only



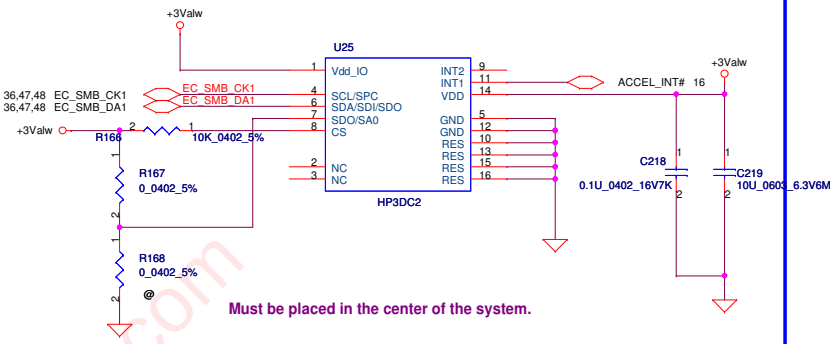
Audio Combo Jack

Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.

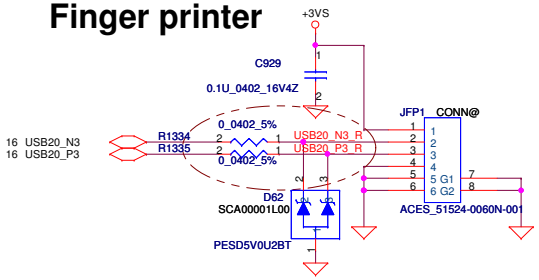
Title	Audio SPK Conn/Jack/MIC	
Size: Custom	Document Number: LA-8711	Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 41 of 57	

ACCELEROMETER



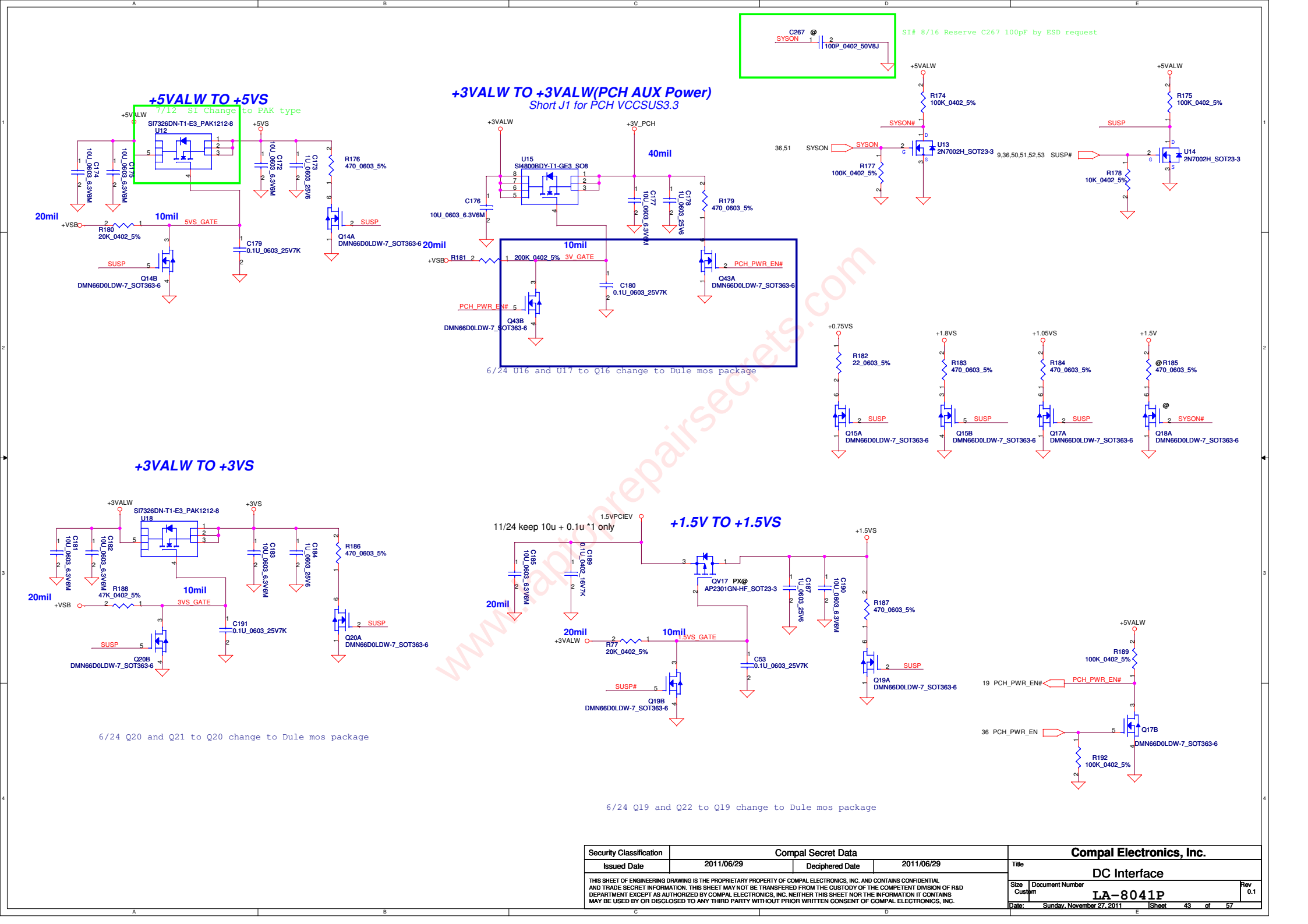
Must be placed in the center of the system.

Finger printer



Security Classification	Compal Secret Data		
Issued Date	2011/11/02	Deciphered Date	2011/11/02

Compal Electronics, Inc.			
Title: TCG/BIOS ROM/PS2/LED/SW			
Size	Document Number: LA-8711		Rev: 0.1
Date: Sunday, November 27, 2011		Sheet 42 of 57	



Security Classification	Compal Secret Data		
Issued Date	2011/06/29	Deciphered Date	2011/06/29

Compal Electronics, Inc.			
Title	DC Interface		
Size	Document Number		Rev
Custom	LA-8041P		0.1
Date:	Sunday, November 27, 2011	Sheet	43 of 57

QC11 (LA-8551P Ver:0.1)

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS_VCCP	+V1.05SP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+VCCP	+VCCP (1.05V) power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII (1.35V OR 1.5V)	ON	ON	OFF
+1.5VS	+1.5VS switched power rail	ON	OFF	OFF
+1.8VS	(+5VALW) to 1.8V switched power rail to PCH	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+LAN_IO	+3VALW to +LAN_IO power rail for LAN	ON	ON	ON*
+3V_PCH	+3VALW to +3V_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V_PCH	+5VALW to +5V_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	B+ to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
G-sensor	0101001b

PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
DDR DIMM1	
Mini Card1	
Mini Card2	
TP module	

EC SM Bus2 address

Device	Address
PCH (Reserve)	1010 0110b

SMBUS Control Table

	SOURCE	BATT	WLAN MIINI1	mSATA MINI2	TP	SODIMM	EC_SMB_CK2 PCH_SMBDATA	PCH_SMBCLK PCH_SMBDATA	G-Sensor	GPU	AMP
EC_SMB_CK1 EC_SMB_DA1	KB930	V							V		
EC_SMB_CK2 EC_SMB_DA2	KB930							V		V	
PCH_SMBCLK PCH_SMBDATA	PCH		@		V	V					V
PCH_SMLCLK PCH_SMLDATA	PCH						V			V	

CLKOUT	DESTINATION
PCI0	PCH_LPBACK
PCI1	PCI_LPC
PCI2	None
PCI3	None
PCI4	None

SATA	DESTINATION
SATA0	m-SATA,JMINI2
SATA1	m-SATA,JMINI1
SATA2	None
SATA3	None
SATA4	None
SATA5	None

USB Port Table

USB 2.0	USB 1.1	Port	1 External USB Port
EHCI1	UHCI0	0	
		1	USB/B (Right Side)
	UHCI1	2	
		3	
	UHCI2	4	
		5	m-SATA
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
	UHCI6	12	
		13	

USB 3.0	Port	1 External USB Port
	0	
	1	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	None	CLKOUTFLEX0	None
	CLKOUT_PCIE1	10/100/1G LAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	USB3.0 FL1009-2Q0		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

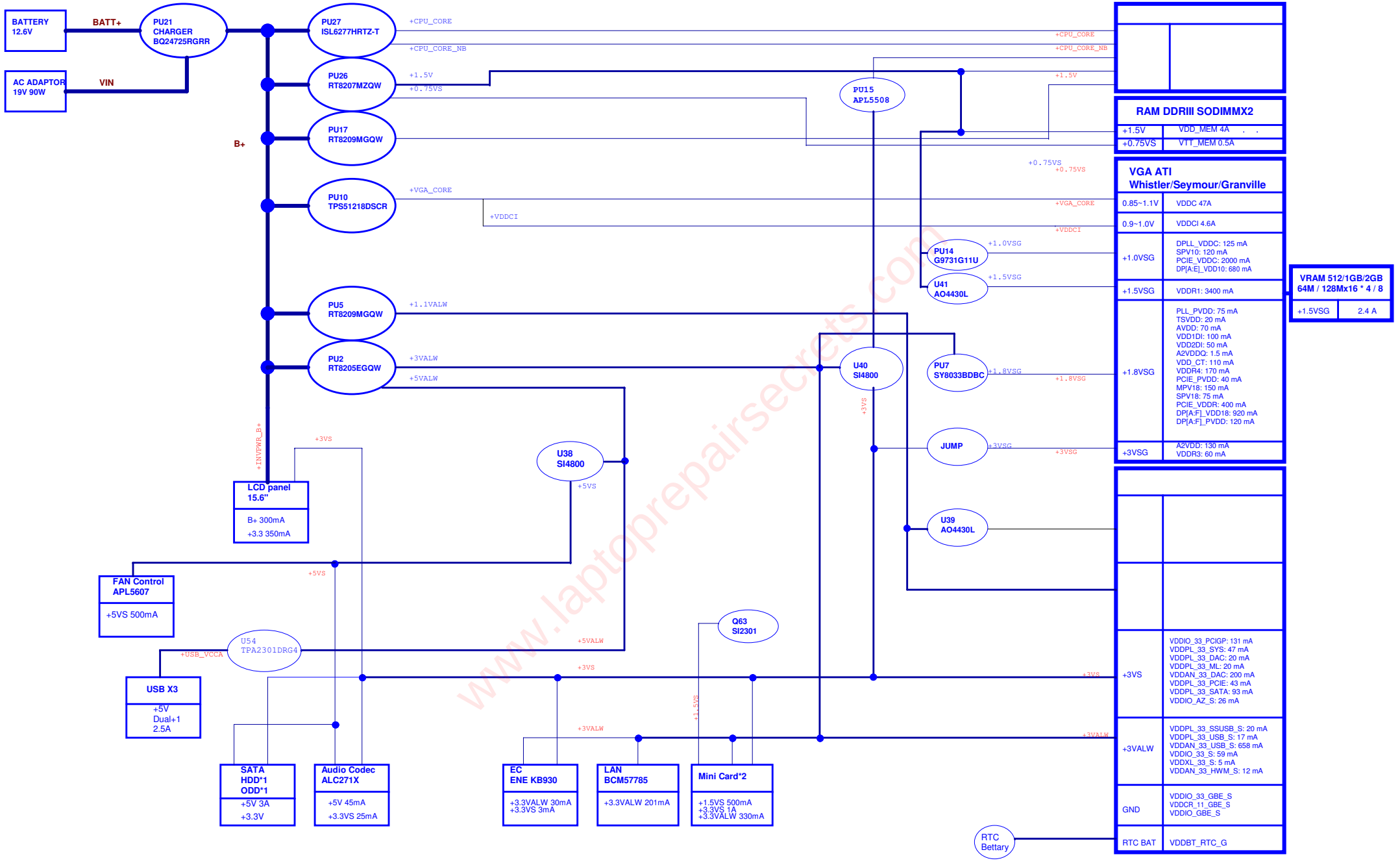
Option	@	CONN@	USB3.0@	
UMA	X	X	V	

Symbol Note :

: means Digital Ground

: means Analog Ground

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/02	Deciphered Date	2011/11/02
Title	Notes List		
Size C	Document Number LA-8711		Rev 0.1
Date: Sunday, November 27, 2011	Sheet 44 of 57		

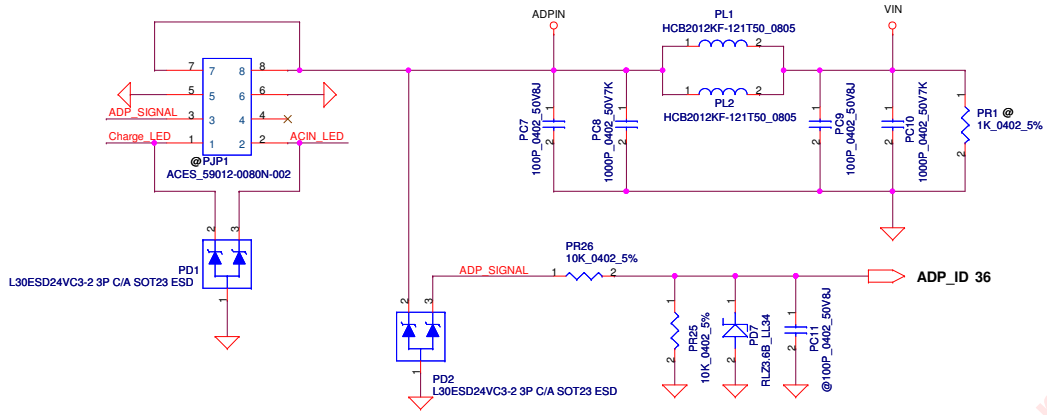


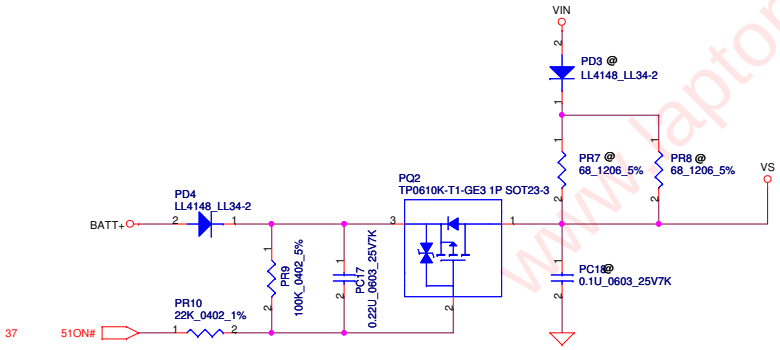
Security Classification	Compal Secret Data		
Issued Date	2011/07/08	Deciphered Date	2015/07/08

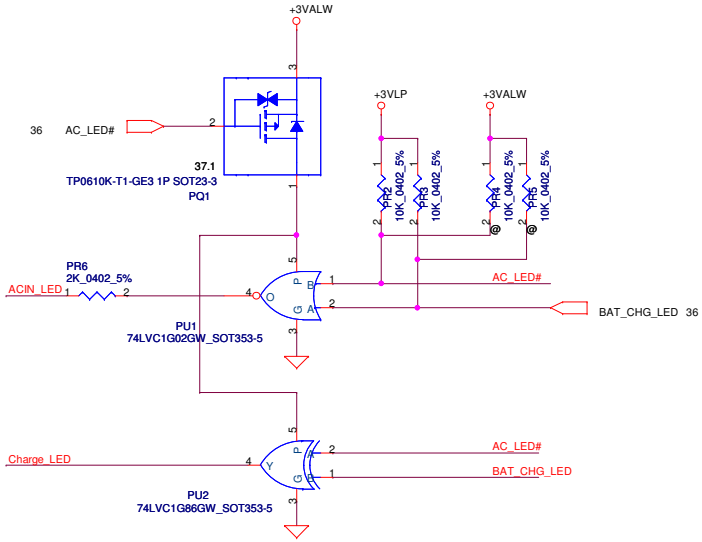
Title: POWER DELIVERY CHART

Size	Document Number	Rev
Custom	LA-8711	0.1

Date: Sunday, November 27, 2011 Sheet 45 of 57







Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.		
Title	PWR- DCIN / Vin Detector	
Size: Custom	Document Number: LA8711P	Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 46 of 57	

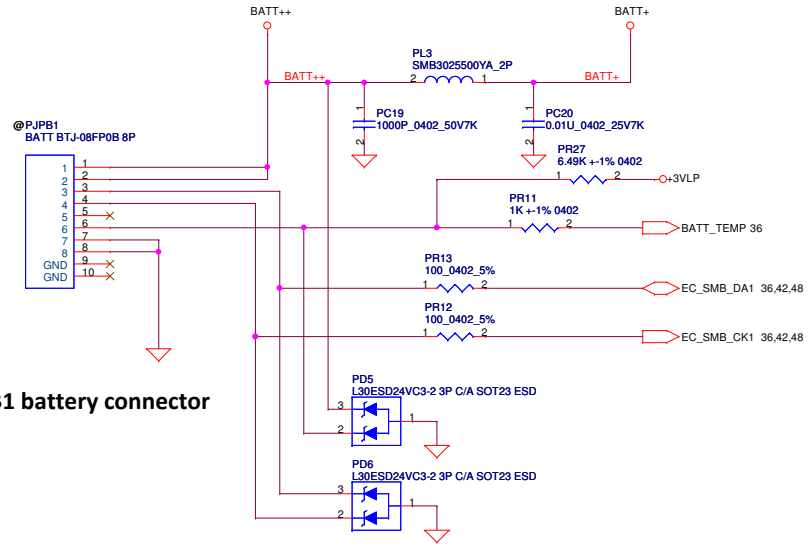
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

For KB9012 --> Remove PU1 circuit, but keep PR25
PH1, PR15, PQ3, PR17,PR18, PR16
VCIN0_PH-->NTC_V
VCIN1_PH-->Turbo_V

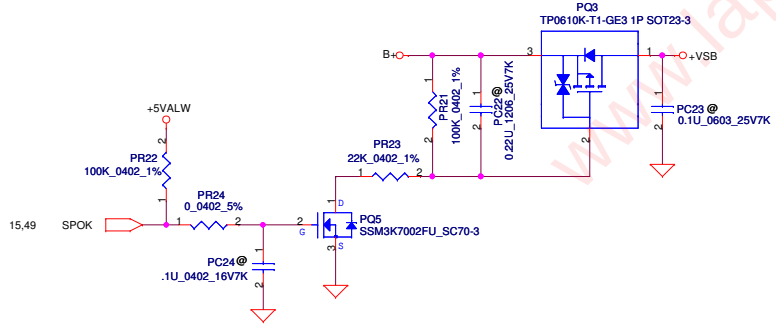
PH1 under CPU botten side :
CPU thermal protection at 90 +-3 degree C
Recovery at 56 +-3 degree C

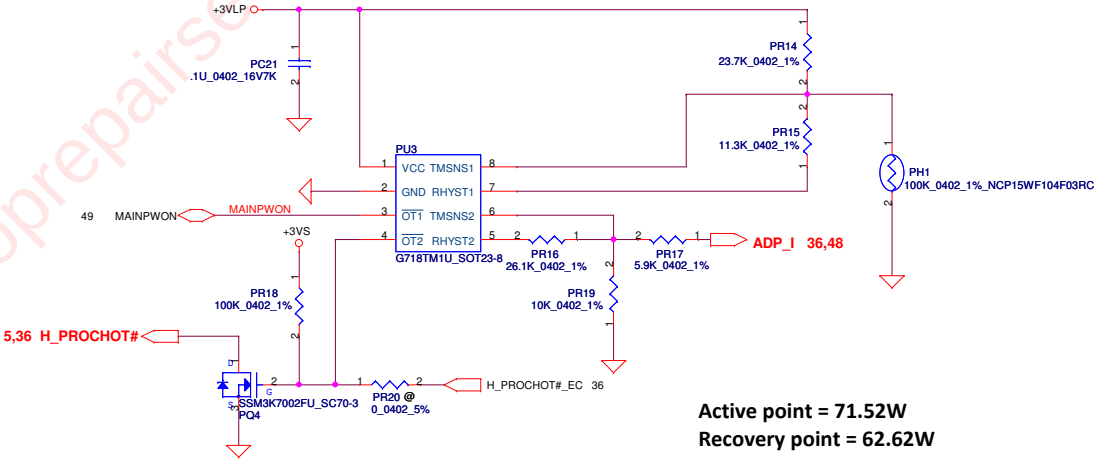
Rset = 3 * Rtmh
Rhyst = (Rset* Rtml) / (3*Rtml - Rset)

Rtmh at 90C = 7.8K, Rtml at 56C = 26.1K
Rset = 3 * 7.8K = 23.4K ==> 23.7K
Rhyst = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K ==> 11.3K



PJPB1 battery connector





Active point = 71.52W
Recovery point = 62.62W

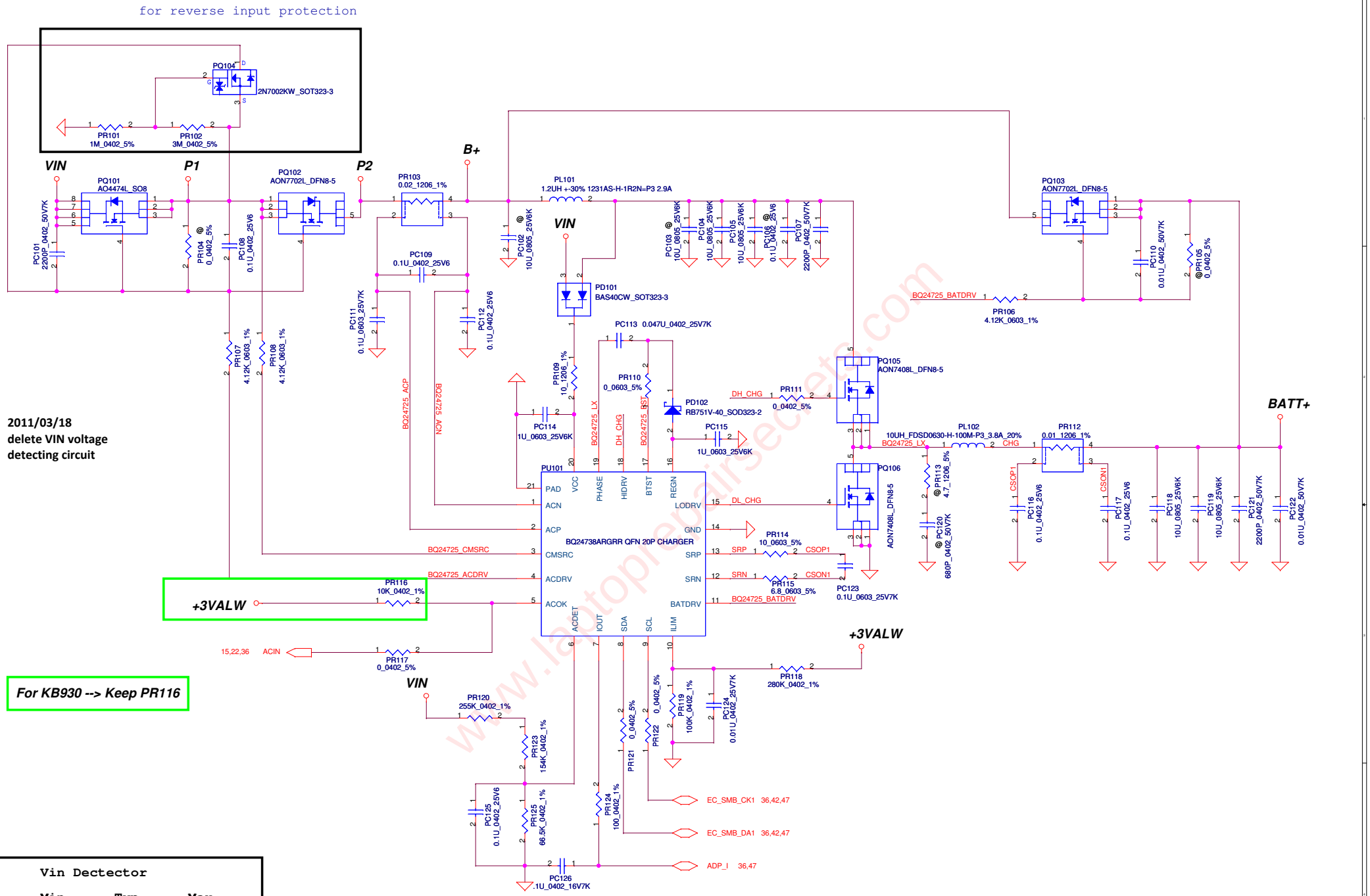
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.

Title: PWR- BATTERY CONN

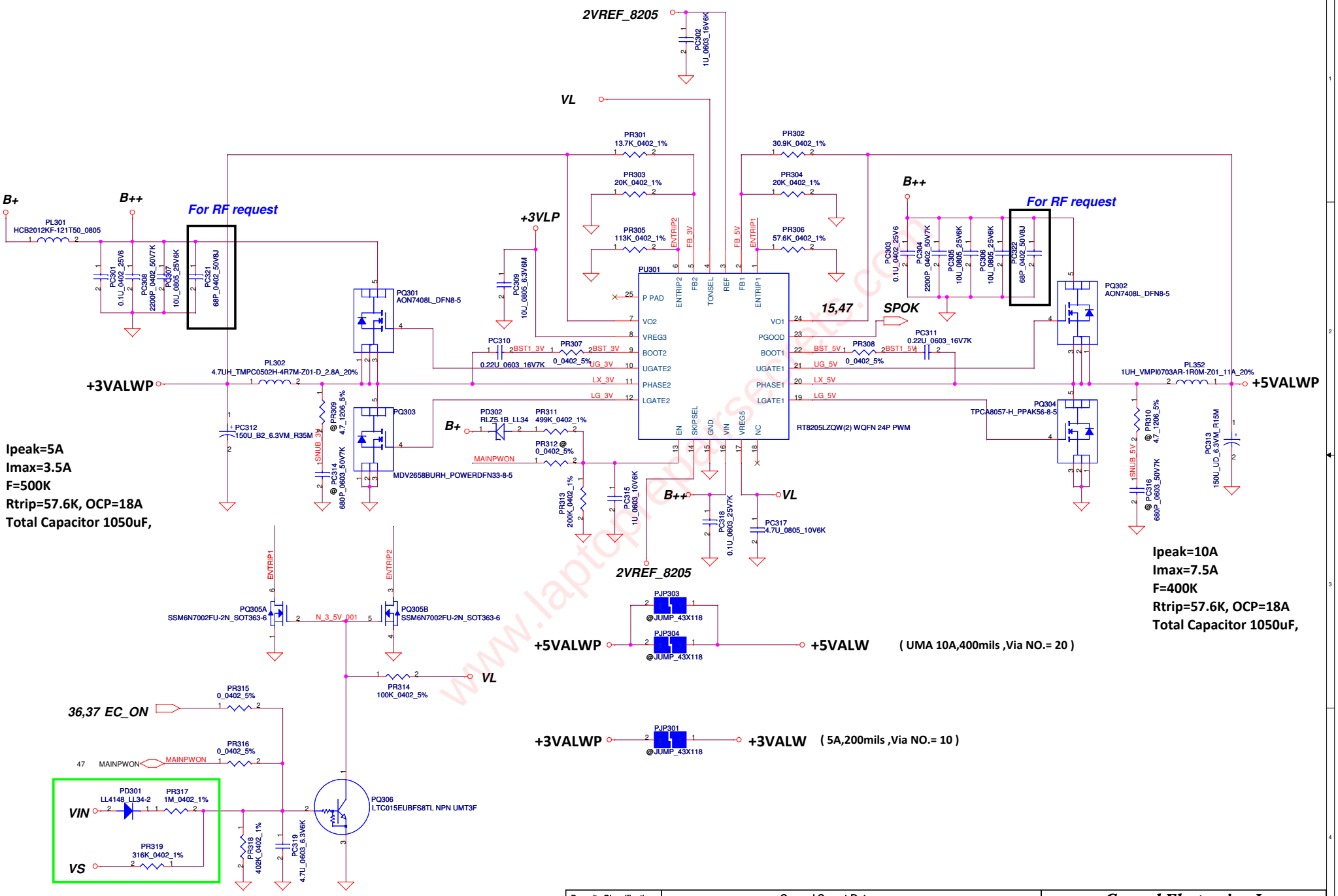
Size: Custom | Document Number: LA8711P | Rev: 0.1

Date: Sunday, November 27, 2011 | Sheet 47 of 57



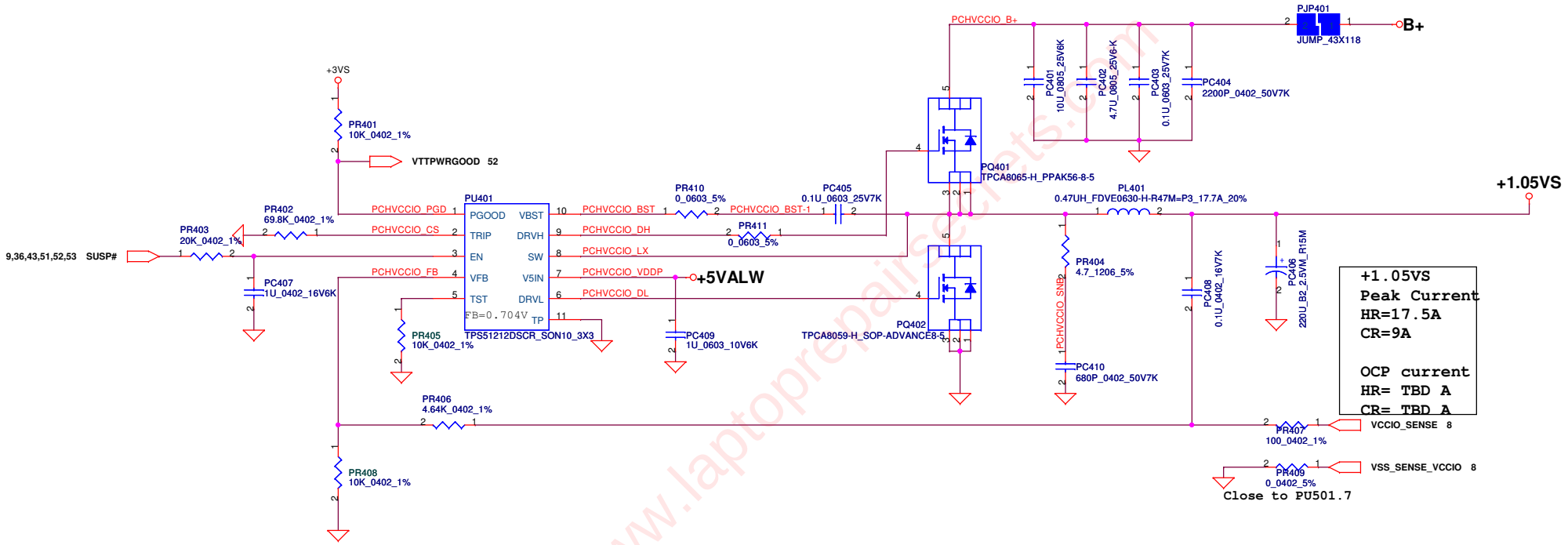
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title	PWR- CHARGER		
Size	Document Number		Rev
	LA-8712P		0.1
Date:	Sunday, November 27, 2011	Sheet	48 of 57



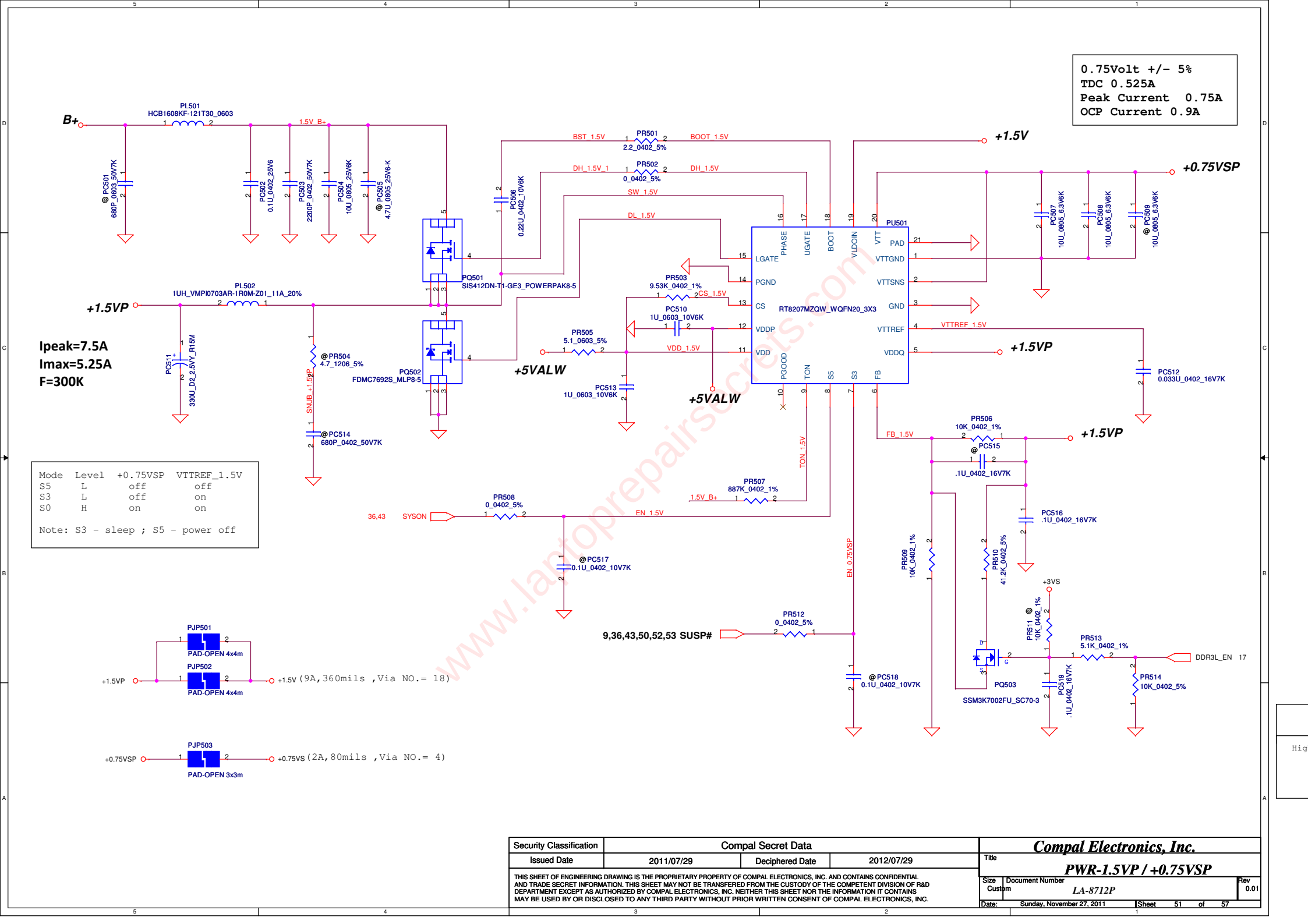
Security Classification	Compal Secret Data		
Issued Date	2011/10/03	Deciphered Date	2014/12/31

Compal Electronics, Inc.			
Title	PWR- 3VALWP/5VALWP		
Size: Custom	Document Number: LA8711P		Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 49 of 57		



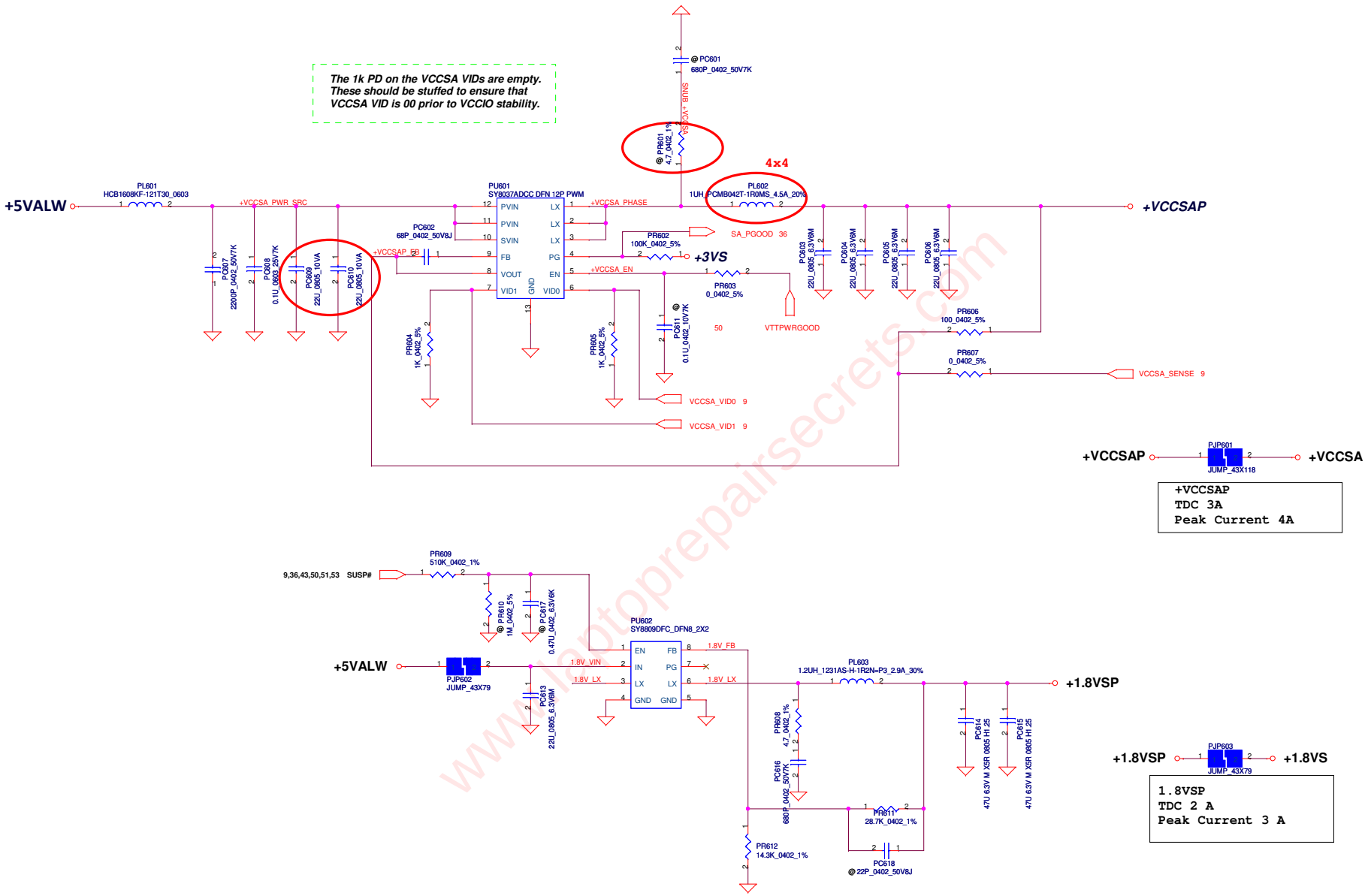
Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.			
Title	PWR-1.05VS		
Size: Custom	Document Number: LA8711P		Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 50 of 57		



Security Classification	Compal Secret Data		
Issued Date	2011/07/29	Deciphered Date	2012/07/29

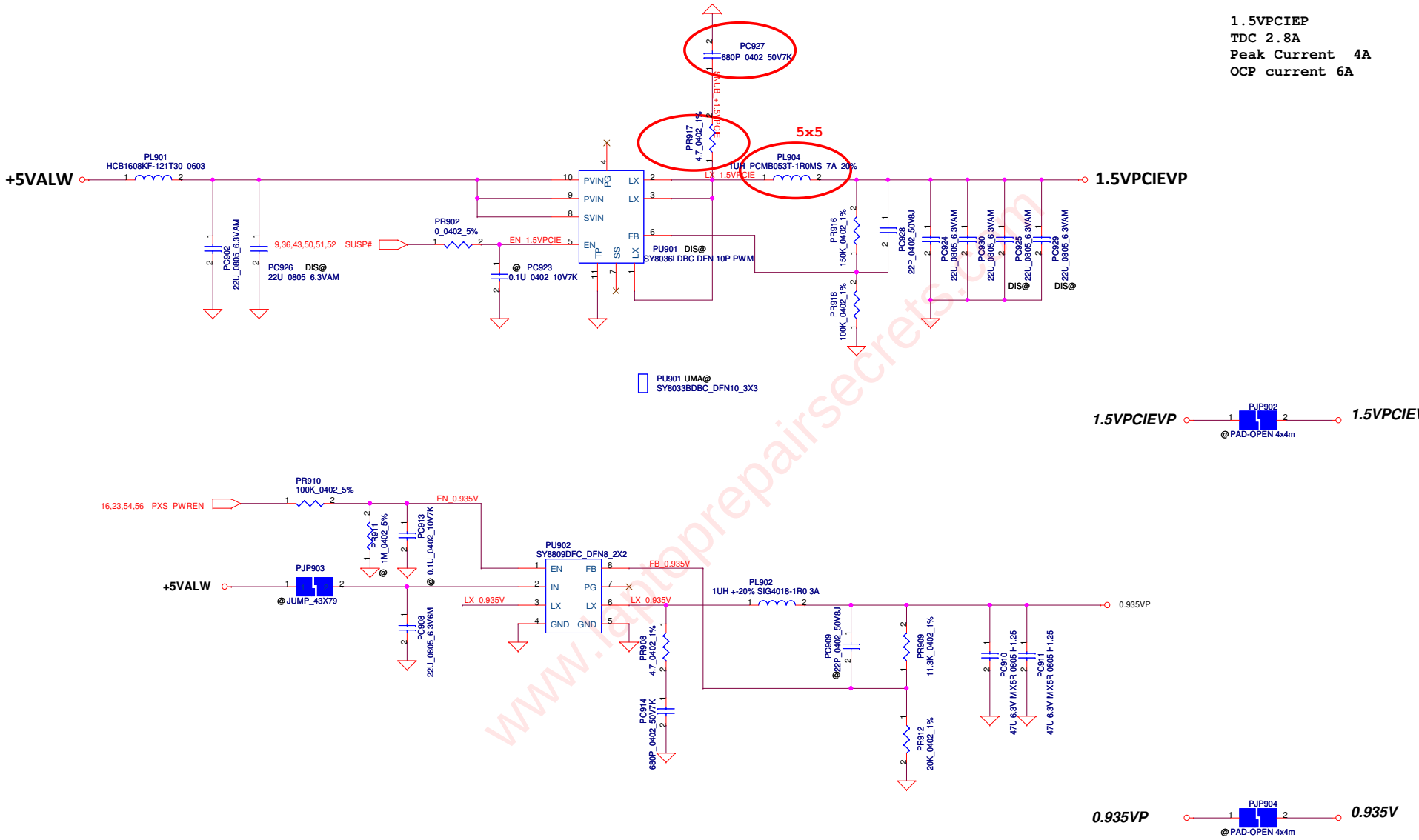
Compal Electronics, Inc.			
Title: PWR-1.5VP / +0.75VSP			
Size: Custom	Document Number: LA-8712P		Rev: 0.01
Date: Sunday, November 27, 2011	Sheet 51 of 57		



Security Classification	Compal Secret Data		
Issued Date	2009/08/23	Deciphered Date	2011/12/31

Compal Electronics, Inc.

Title	PWR-VCCPP/1.8VSP	
Size: Custom	Document Number: LA8711P	Rev: 0.1
Date: Sunday, November 27, 2011	Sheet 52 of 57	



Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

Title: **+1.5VPCIE/0.935V**

Size	Document Number	Rev
	LA8711P	0.2

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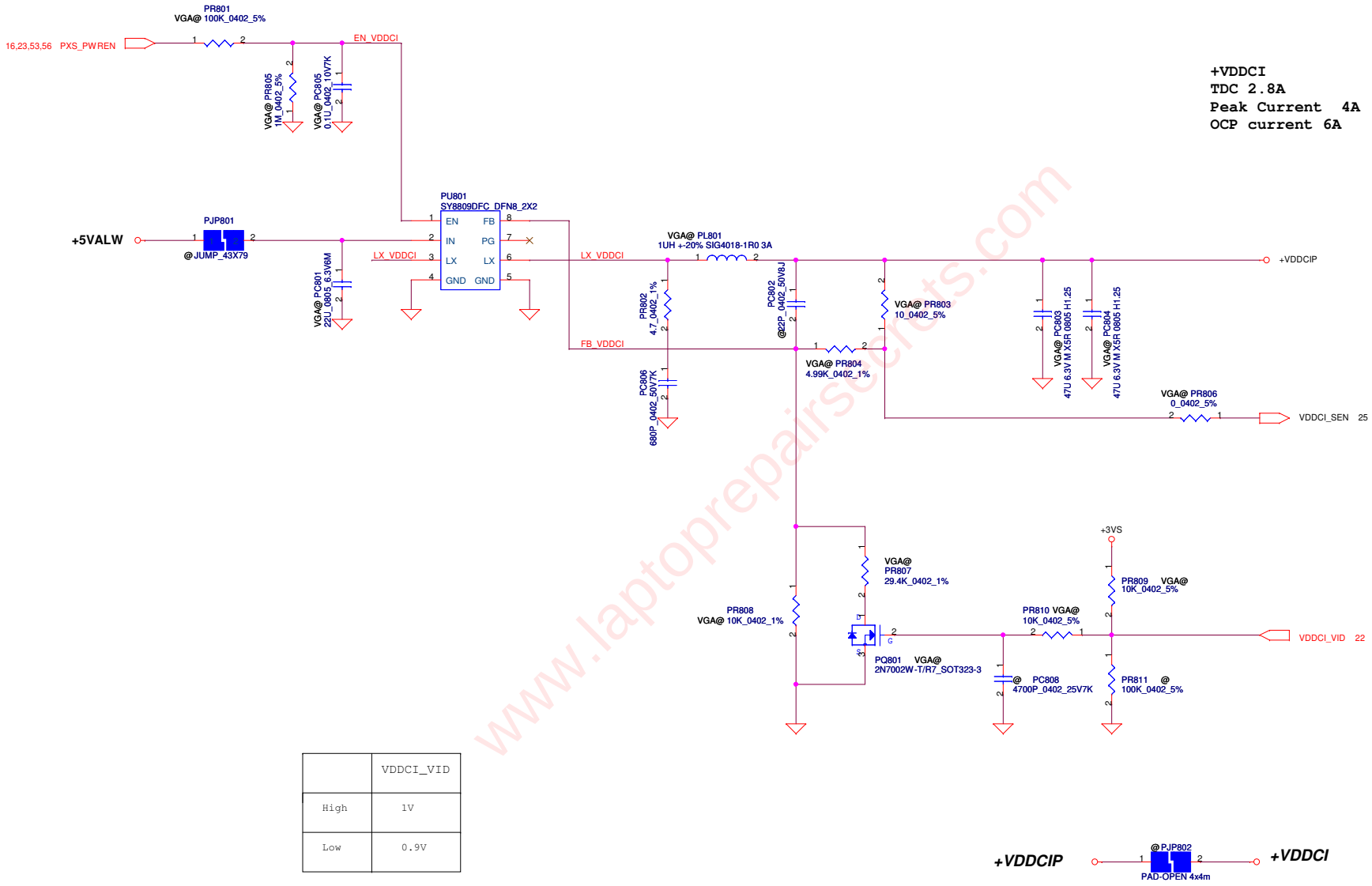

+VDDCI
TDC 2.8A
Peak Current 4A
OCP current 6A

	VDDCI_VID
High	1V
Low	0.9V

Security Classification	Compal Secret Data		
Issued Date	2011/08/16	Deciphered Date	2012/08/15

Compal Electronics, Inc.

Title: +VDDCIP

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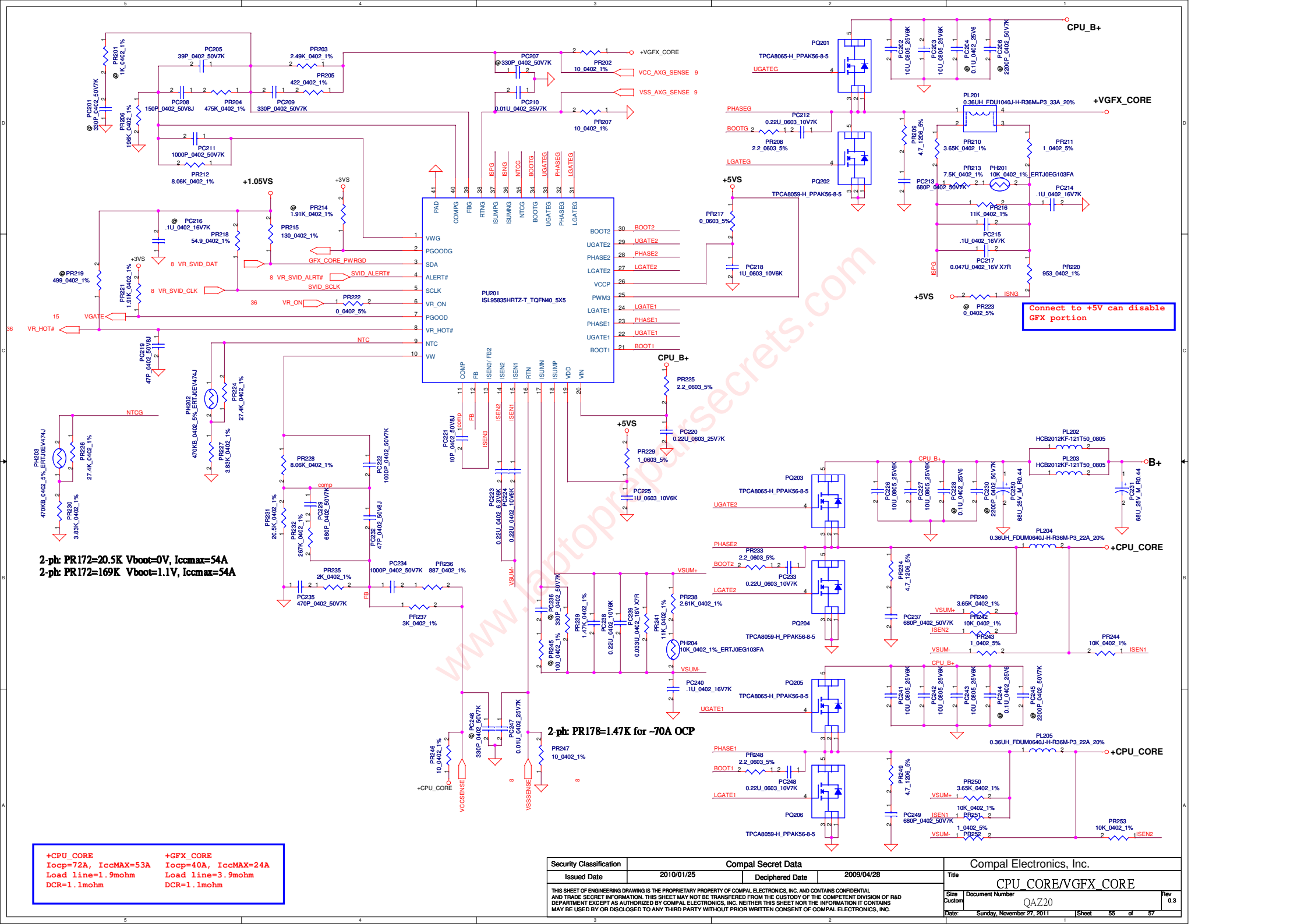
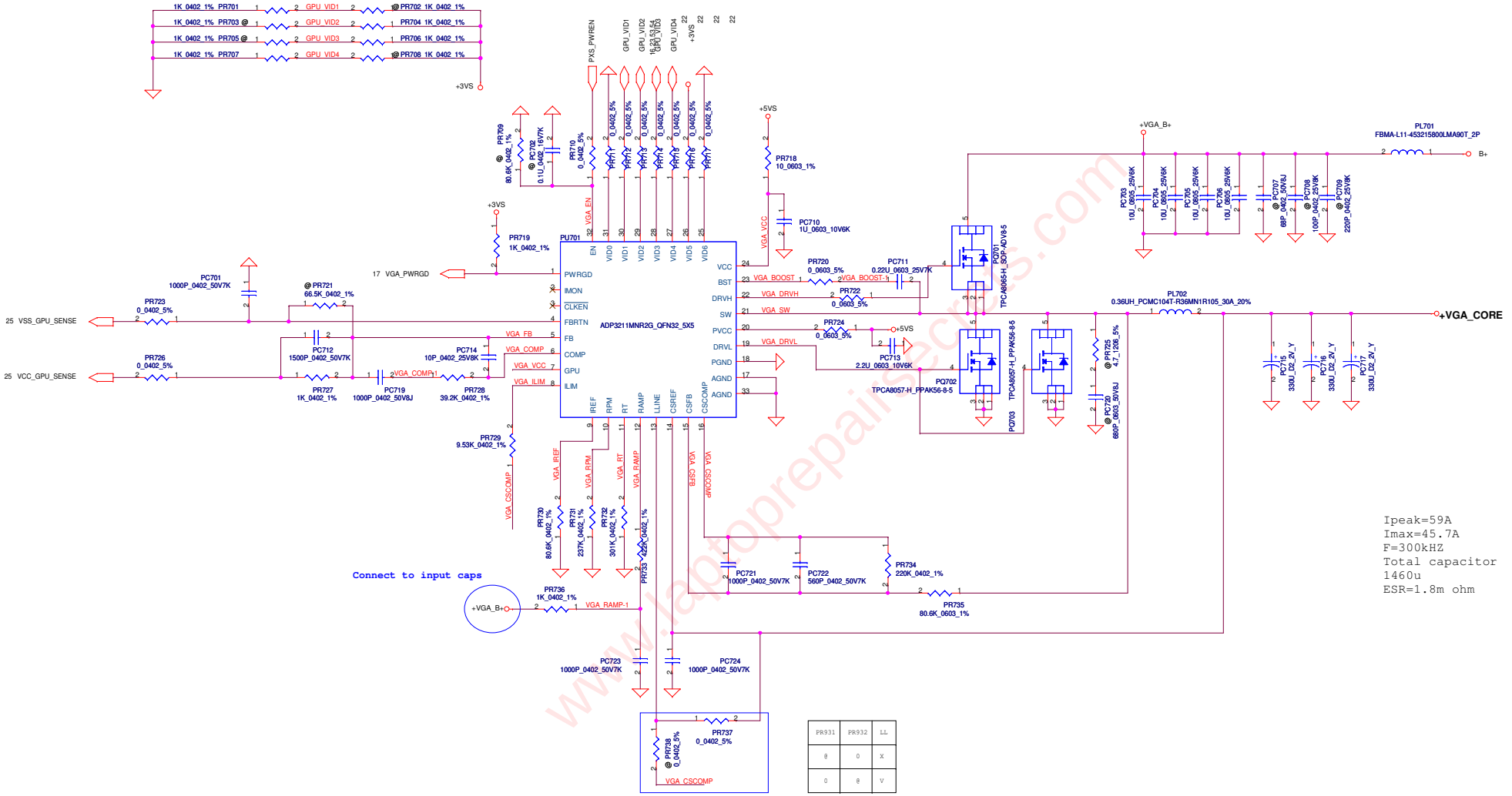
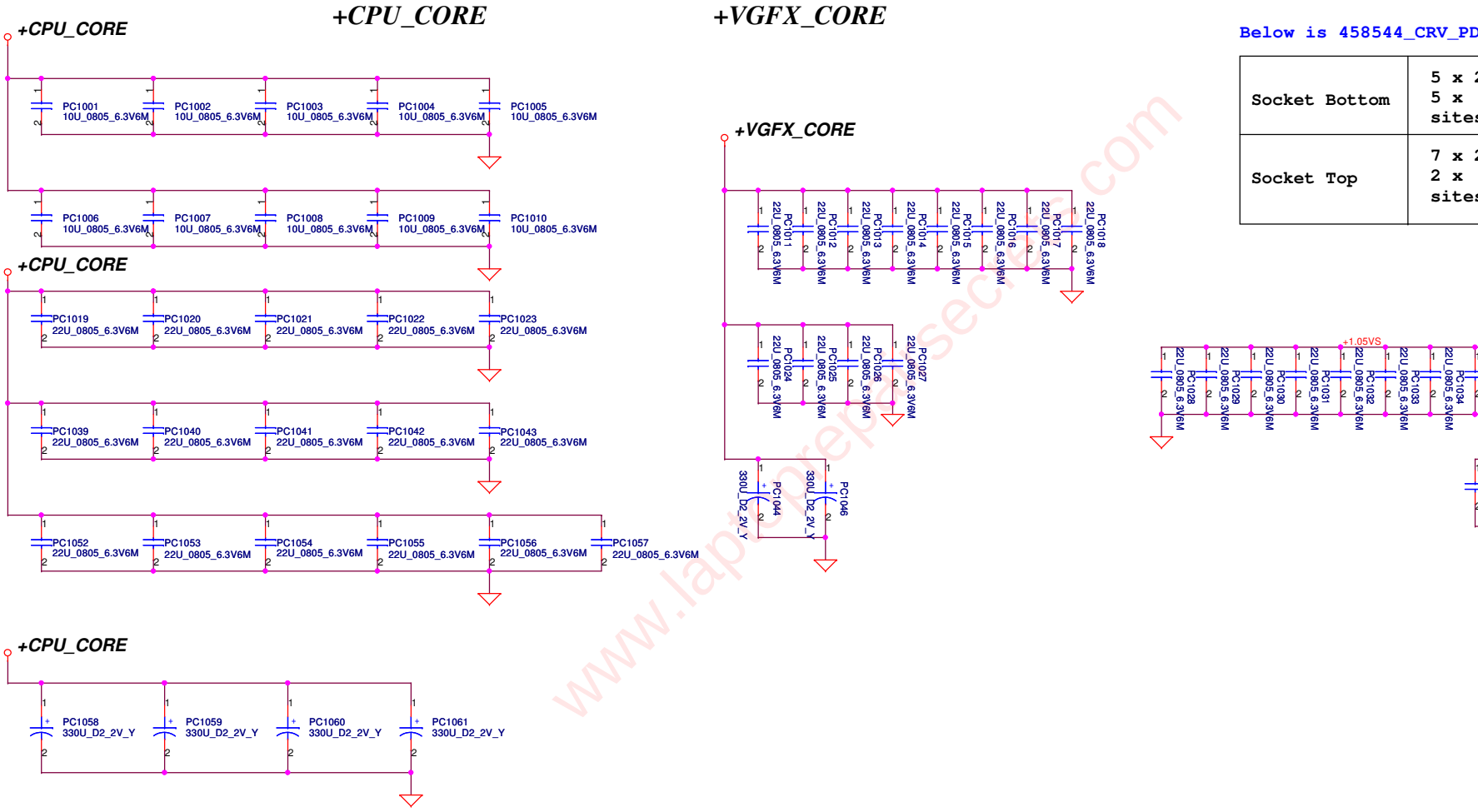




Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

Compal Electronics, Inc.			
Title	+VGA_COREP		
Size	Document Number	LA-8712P	Rev 0.3
Date: Sunday, November 27, 2011	Sheet 56 of 57		



+CPU_CORE

+VGFX_CORE

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PWR - PROCESSOR DECOUPLING

Size	Document Number	Rev
	LA8711P	0.1

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